International Research Journal in Global Engineering and Sciences. (IRJGES)
ISSN : 2456-172X | Vol. 2, No. 4, December - February, 2018
Pages 63-68 | Cosmos Impact Factor (Germany): 5.195
Received: 02.02.2018 Published : 28.02.2018

Analog Low Noise Amplifier Circuit Design and Optimization

Sathyanarayana, R.Siva Kumar. M, Kalpana.S
Dhanalakshmi Srinivasan College of Engineering and Technology, Tamil Nadu, India

Abstract—A style and optimisation of three gigahertz single concluded frequence (RF) Low Noise Amplifier(LNA) for wireless applications mistreatment commonplace UMC zero.18µm CMOS technology is reportable. planning of RF circuit elements could be a difficult job, since even when performing arts extended calculations and finding parameter values it's less guarantee that the look performs of course. visible of this the optimisation tool; moralist Non-Dominated Sorting Genetic rule (NSGA-II); has been used to induce the optimized beginning values of elements within the style. The obtained NSGA-II parameters were simulated mistreatment Cadence Spectre- RF machine. The designed Low Noise electronic equipment achieves an influence gain of fourteen.49 decibel and a minimum Noise Figure of one.897 decibel is achieved. It dissipates eleven.7 mW of power out of one.8 V supply.

Index Terms—NSGA-II rule, LNA, noise figure, power gain.

I. INTRODUCTION

The expansion of multimedia system services and applications in digital information transmission has junction rectifier to ever increasing demands of wireless communication systems [1]. New standards are being approved and designed so as to faucet the exploding market, several of those new standards try and connect devices and or appliances within the home mistreatment lower performance radio transceivers. Also, recent years have intimate with explosive growth within the frequence /microwave semiconductor trade thanks to the proliferation of a bunch of applications. Single-chip Bluetooth devices are already accessible and similar integration is probably going to be achieved in cellular telephones and wireless networking in close to future. frequence elements are the essential building blocks of transceivers operative in gigahertz frequency vary. planning of RF circuit element desires heap of effort. when performing arts extended calculations and finding the parameter values it's not warranted that the circuit performs of course. In frequence Integrated Circuits (RFIC), Low Noise Amplifiers are thought of as magic box thanks to their unsure response with higher frequencies. thanks to twin of input resistance and output resistance most power transformation isn't doable. For planning of the circuit, input and output resistance circuit, we want to style a passive filter with optimized element values. optimisation of the element price could be a time overwhelming job. visible of this a CAD tool mistreatment Non-Dominated Sorting Genetic rule (NSGA-II) has been used. the look goal is developed as associate objective operate. Some approximations and estimations on the look parameters are created so as to satisfy the necessity of the genetic rule. several applications of genetic rule and optimisation of LNA parameter by binary coded genetic rule is reportable in [2], [3]. during this paper we tend to are presenting optimisation for single concluded LNA mistreatment real coded genetic rule. In Section II;

International Research Journal in Global Engineering and Sciences. (IRJGES)
ISSN : 2456-172X | Vol. 2, No. 4, December - February, 2018
Pages 44-49 | Cosmos Impact Factor (Germany): 5.195
Received: 24.02.2018 Published : 27.02.2018

transient introduction of Non-Dominated Sorting Genetic rule is given. In Section III analysis and style downside of low noise electronic equipment is bestowed, in Section IV style objective and constrains optimisation of LNA is mentioned. In Section V simulation result and discussion is bestowed. Scope and limitation of the NSGA-II has been mentioned in Section VI and eventually Section VII concludes the paper.

II. **NON-DOMINATED SORTING GENETIC**

Genetic rule and Genetic algorithms [3], [4] are search techniques utilized in computing to seek out true or approximate solutions to go looking or optimisation issues. it's supported ideas of survival of the fittest, replica and mutation and has been used extensively in optimisation issues. It is classified in 2 sets reckoning on style of writing of the members; one is binary coded and second is real coded [3]. In past few years GA has undergone many developments developing its options, time interval etc, some such developments are Multi Objective Genetic rule (MOGA) [5], [6], moralist Non Dominated Sorting Genetic rule [3].

III. **ANALYSIS OF LOW NOISE**

Electronic equipment the first a part of this section is predicated on the literature survey and concludes with own design. joined of the essential elements, Low Noise Amplifiers (LNAs) for wireless applications have attracted important analysis interest and numerous approaches to the look of narrowband LNAs (operating below three GHz) and broadband LNAs (operating higher than three GHz) are planned antecedently [7]-[15] and as shown in Fig. 1(a)- Fig. 1(d). Distributed amplifiers [7] will offer terribly giant information measure thanks to their distinctive gain-bandwidth trade-off. However, giant power consumption and chip space create them unsuitable for typical low –power, low value wireless applications. Common-gate amplifiers [8], [9] exhibit wonderful wide band input matching, however suffer from a comparatively giant noise figure (NF). Narrow-band LNAs like associate inductively degenerated common-source electronic equipment may also be reborn into a broadband one by adding a broadband input matching network [10]. However, the insertion loss of the passive input matching degrades the NF chop-chop with frequency. Resistive-feedback amplifiers [11]-[14] have superb broadband input matching characteristics. However, low NF and low power consumption are often hardly achieved at the same time across an outsized frequency vary. In [15], noise cancellation technique is employed to relax this trade-off in resistive feed-back amplifiers. A typical LNA should fulfill many difficult needs. The LNA should offer a decent input matching over a band quite five hundred Mc. A high gain is additionally most popular to amplify the week signals at the receiver and to beat the noise effects from the next stages. additionally, the noise figure of the LNA should be low (< three dB) since it plays a serious role in shaping the receiver's sensitivity. Moreover, the LNA conjointly must be power economical and physically tiny to avoid wasting power and cut back the value, severally.

International Research Journal in Global Engineering and Sciences. (IRJGES)
ISSN : 2456-172X | Vol. 2, No. 4, December - February, 2018
Pages 44-49 | Cosmos Impact Factor (Germany): 5.195
Received: 24.02.2018 Published : 27.02.2018

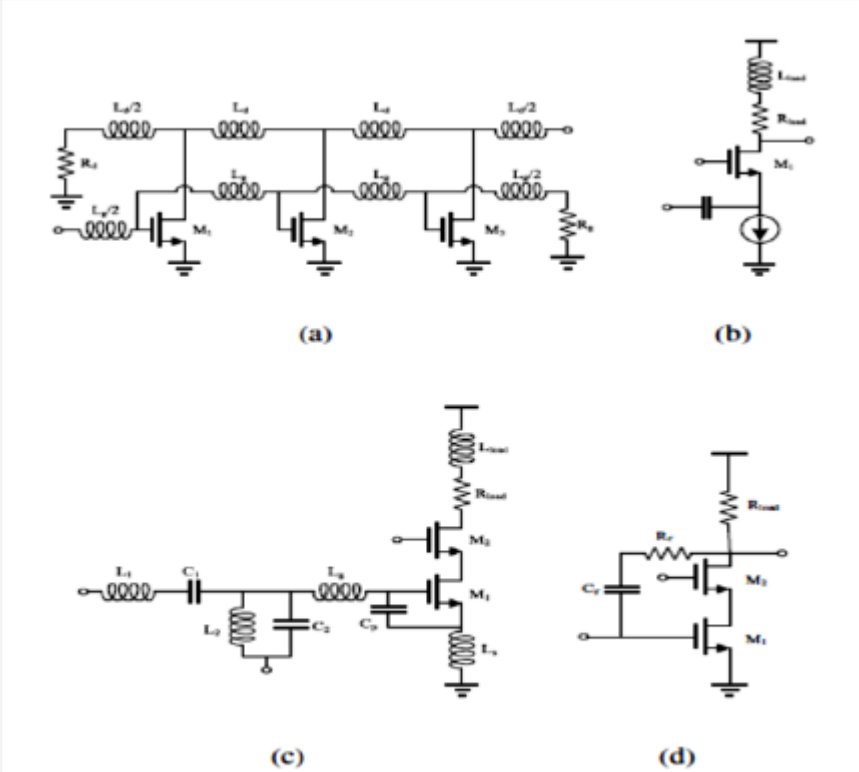

Fig. 1. Various LNA topologies (a) distribute amplifier, (b) common gate, (c) inductive degeneration, (d) resistive feedback.

Using the available literature as references, the specific goal here is to achieve a low-power (<11 mW) operation, medium gain (power gain >10 dB) LNA, a small noise figure (<2.5 dB). An inductively degenerated LNA configuration is proposed, as shown in Fig. 2(a).

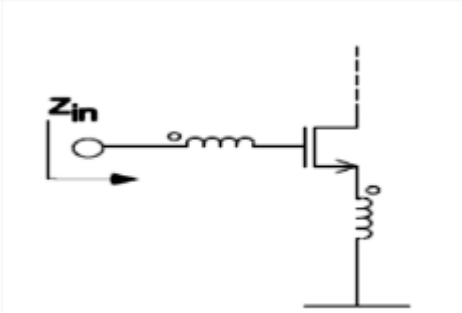

Fig. 2(a). Inductive source degeneration.

International Research Journal in Global Engineering and Sciences. (IRJGES)
ISSN : 2456-172X | Vol. 2, No. 4, December - February, 2018
Pages 44-49 | Cosmos Impact Factor (Germany): 5.195
Received: 24.02.2018 Published : 27.02.2018

Inductive degeneration improves the linearity of the amplifier. The input impedance can be derived from the small signal analysis [16] of Fig. 2(b). By looking into the input side of Fig. 2(b), input impedance Zin can be:

$$Z_{in} = s(L_s + L_g) + R_g + \frac{1}{sC_{gs}} + (\frac{g_m}{C_{gs}})L_s \qquad (1)$$

where Ls, Lg are the source and gate inductances, respectively; Rg is the transistor gate resistance, Cgs is the transistor gate-to-source capacitance; gm is the transistor trans-conductance. The inductor parasitic resistance is ignored here. Input match requires that at the resonance frequency of the circuit, the impedance of the input stage is purely real and should be equal to 50.

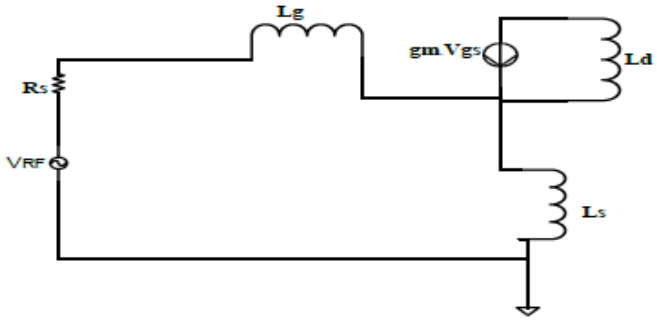

Fig. 2(b). Small signal equivalent of Fig. 2(a).

It follows that:

$$R_g + (\frac{g_m}{C_{gs}})L_s = 50 \qquad (2)$$

where ω_0 is the resonance frequency (rad/s), and

$$j\omega_0(L_s + L_g) + \frac{1}{j\omega_0 C_{gs}} = 0 \qquad (3)$$

The noise factor (F) is defined as [7], [8]:

$$F = 1 + \frac{R_l}{R_s} + \frac{R_g}{R_s} + \frac{\gamma}{\alpha} g_m R_s (\frac{\omega_0}{\omega_T})^2 \qquad (4)$$

$$NF = 10 \cdot \log_{10}(F)$$

where unity frequency:

$$\omega_T = \frac{g_m}{C_{gs}}, \ \alpha \equiv \frac{g_m}{g_{d0}},$$

International Research Journal in Global Engineering and Sciences. (IRJGES)
ISSN : 2456-172X | Vol. 2, No. 4, December - February, 2018
Pages 44-49 | Cosmos Impact Factor (Germany): 5.195
Received: 24.02.2018 Published : 27.02.2018

Rs: source resistance, Rl : series resistance of inductors, Rg : gate resistance, : the thermal noise coefficient, 0 : the resonance frequency, gm: transistor trans-conductance. For a source inductively degenerated LNA in Fig. 2, we could put a lower bound on the trans-conductance of the input transistor to ensure that the final designed LNA can provide a reasonable gain [9] .

$$A_V = G_m Z_{eq} = \left(\frac{1}{jw_0 L_s}\right)\left(\frac{jw_0 L_1}{1 - w_0^2 L_1 C_0}\right) \qquad (5)$$

In order to formulate a geometric programming problem, we have to do some transformation and introduce new variable to satisfy the requirement of geometric programming on the objective and constrains. Inequality constrains and the objective function must be in the form of polynomial, equality constrains must be in the form of monomial. Here noise figure and gain is formulated for low noise amplifier. For low noise amplifier, Objective function of Noise Figure can be formulated as:

$$F = F_{\min} + 50 \times R_n \times (0.02 - G_{opt})^2 \qquad (6)$$

where, $F_{\min} = \dfrac{1 + 2 \times W_0 \times \sqrt{\delta \times \gamma \times (1 - C^2)}}{Wt \times \sqrt{5}}$

$$Rn = \frac{\gamma}{\alpha \times G_m}$$

$$Gopt = \alpha \times W_0 \times Cgs \frac{\sqrt{\delta \times (1 - C^2)}}{5 \times \gamma}$$

Objective function of the Gain of LNA can be formulated as:

$$Gain = \frac{W_t \times R_{load}}{W_0 \times 2 \times R_{load}} \qquad (7)$$

And objective function of power consumption has been formulated as:

$$P_{DC} = I_D \times V_{DC} \qquad (8)$$

where,

$$I_D = \frac{\mu_n \times C_{ox} \times Width \times V_{od}^{\ 2}}{2 \times ChannelLength}.$$

International Research Journal in Global Engineering and Sciences. (IRJGES)
ISSN : 2456-172X | Vol. 2, No. 4, December - February, 2018
Pages 44-49 | Cosmos Impact Factor (Germany): 5.195
Received: 24.02.2018 Published : 27.02.2018

IV. CONCLUSION

This paper shows that the optimization of RF Circuits is possible with real coded genetic algorithm. It is found that real coded Multi-Objective Genetic Algorithm has many advantages over binary coded genetic algorithm. Non-Dominated Sorting Genetic Algorithm is used for optimization tool, which is giving comparative results with design software simulation like Cadence Spectre tool. In this paper it is shown that the Low Noise Amplifier can be designed for parameter for noise figure of 1.897dB and power gain of 14.49dB.In future the NSGA-II optimization tool can be used to extend for 3-5GHz LNA design for wideband wireless RF system. Thus the design tool is useful in finding circuit element values quickly reducing the RF circuit designer time.

REFERENCES

[1] Federal communications commission. [Online]. Available: http://www.fcc.fov
[2] M. Chu and D. J. Allstot, "Elitist nondominated sorting genetic algorithm based RF IC optimizer," IEEE Transaction, vol. 52, no. 3, pp. 535-545, 2005.
[3] K. Deb, "Multi-objective optimization," Multi-objective Optimization using Evolutionary Algorithms, pp. 13-46, 2001.
[4] D. E. Goldberg and J. H. Holland, "Genetic Algorithms in Search, Optimization, and Machine Learning," Machine learning, vol. 3, no. 2, pp. 95-99, 1988.
[5] N. Chaiyaratana and A. M. S. Zalzala, "Recent development in evolutionary and genetic algorithms: Theory and applications," in Proc. 2nd International Conference on Genetic Algorithms in Engineering Systems: Innovations and Applications, 1997, pp. 270-277.
[6] K. Deb, "Single and multi-objective optimization using evolutionary algorithms," presented at KanGAL Report No. 2004002, February, 2004.
[7] B. M. Ballweber, R. Gupta, and D. J. Allstot, "A full integrated 0.5-5.5 GHz CMOS distributed amplifier," IEEE Journal of Solid State Circuit, vol. 35, no. 2, pp. 231-239, Feb. 2000.
[8] C. F. Liao and S.-I. Liu, "A broad band noise cancelling CMOS LNA for 3.1-10.6GHz wireless receivers," IJSSCC, vol. 42, no. 2, pp. 329-339, Feb.200
[9] R. Gharpure, "A broadband low noise front end amplifier for ultra wideband in 0.13um CMOS, " IEEE Journal of Solid State Circuits, vol. 40, no. 9, pp. 1983-1986, Sep. 2005.
[10] W. H. Chen, G. Liu, B. Zdravko, and A. M. Niknejad, "A highly linear broadband CMOS LNA employing noise and distortion cancellation," in Proc. 2007 IEEE Symposium on Radio Frequency Integrated Circuits (RFIC), 2007, pp. 61-64.
[11] A. Bevilacqua and A. M. Niknejad, "An ultra wide band CMOS LNA for 3.1-10.6 GHz wireless receivers," IEEE Journal of Solid-State Circuits, vol. 39, no. 12, pp. 2259-2268, 2004.
[12] C. W. Kim, M. S. Kang, P. T. Anh, H. T. Kim, and S. G. Lee, "An ultra-wide band CMOS low noise amplifier for 3-5 GHz UWB System," IEEE J. Solid State Circuits, vol. 40, no. 2, pp. 544-547, Feb. 2005.