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Grid Connected Multilevel Inverter TopologySuitable for Solar PV Applications with Varying Irradiance

B. Keerthana, P.Karthik, D.Sureshkumar, A.Sugunaya
Assistant Professor
Department Of Electrical & Electronics Engineering, A.R Engineering College,Villupuram
Email: Keerthanagow10@gmail.com

***Abstract*—**A new asymmetrical multilevel inverter topology is reported that is capable to operate satisfactorily with wide varia- tion in dc-link voltage, while feeding power to the ac grid. A topo-logical building block is first introduced that has one full-bridge inverter connected in series with a level doubling network. Follow-ing this, the interconnection of such building blocks is attempted to increase the number of levels at the output voltage waveform. The investigation reveals that for a three-phase system, a converter configuration with two such building blocks is capable to generate a nominal asymmetry of 14:7:2:1 using only four voltage sources. In solar Photovoltaic (PV) applications, one main source may be fed by PV array and the other three auxiliary sources may be fed through separate dc/dc converters, each having power rating of 3.2% of the peak power rating of PV arrays. The proposed con- verter can generate 3097 space vectors. Asymmetrical hexagonal decomposition is modified (to ensure satisfactory operation of LDN and to eliminate any dc component in the phase voltage waveform) to control such converter. The converter is extensively simulated in MATLAB/Simulink. A solar PV system of 9.4 kWp available in the laboratory is used to feed power to the grid at different irradiance. Simulation results match well with the prototype experiments con-firming the usefulness of the proposed topological alternative for solar PV applications.

Index Terms—**Gridconnected photovoltaic inverter, central inverter, multilevel inverter, level doubling network, inverter topology.**

INTRODUCTION

PHOTOVOLTAIC inverter is in the core of a grid connected Photovoltaic (PV) system. Leakage current (due to stray capacitance between the terminal and frame of PV module) is a key issue that influences selection of topology for such inverters.

Energy yield from a PV power plant depends on both *efficiency*and *reliability* of these inverters [1]. While a great attentionis paid to increase the efficiency to enhance energy capture, a considerable loss in the evacuation of power is observed due toinverter failure. The main reason for inverter failure is high fre-quency switching of few hundreds of ampere of output current.This current could be reduced by elevating the voltage level ofthe PV arrays. However, this is not recommended due to severalissues such as potential induced degradation (PID) [2], dielec- tric breakdown [3] etc., those limit the PV array voltage to a maximum of 600–900 volts. This leaves no other alternative but to have a central inverter with rated current of hundreds of ampere.

The key design constraints for a PV inverter are:

1) Leakage current must be below recommended standards,
2) Peak dc bus voltage has to be limited to 600–900 V,
3) Power quality has to be maintained as per grid code,
4) The solar park should not inject unbalanced current in tothe grid.

To satisfy the above requirements, many PV converter topolo- gies came up in last three decades. This section briefly highlights the merits and limitations of few potentially important topolo- gies. To increase the

efficiency, it was attempted to reduce iron losses by removing the transformer. Many transformer- less topologies were evolved [4]. None of these topologies are suitable for central inverter applications. Neutral point clamped(NPC) structures were proposed and analyzed for transformer-less PV inverters in [5]–[7]. However, as shown in [8], NPC structures also require due attention to mitigate leakage current in its three-phase version, which reduces its peak voltage by a factor of 0.866 rejecting certain space vectors. This introduces additional loss in filter/coupling inductor. Moreover, any stray inductance in the neutral line may cause leakage current higherthan the limit.

Z-source inverters or its derived topologies [9]–[11] are re- ported for solar PV applications. This has the advantage of hav- ing higher range of MPPT operation. However, this is achieved at the cost of high frequency switching. Additional loss of energy is obvious in the passive components (mainly in the inductors)in these converter topologies.

The other approach to develop grid connected PV inverter is to explore cascaded multilevel inverter topologies to main- tain power quality with reduced switching and inductor losses [12]–[18]. In [12]–[14], cascaded H-bridge is directly used as PV inverter. Due to inter-array capacitance, these topologies will have leakage current even in case of transformer isolation from the grid. This issue is addressed in [15] by using com- mon mode choke or by providing a parallel lower impedance path to effectively bypass leakage current from mounting struc- ture. Isolated high-frequency-link is used in [16] for utility scale transformer-less PV inverter. A major concern for this topology is reliability: large numbers of high frequency links are supposed to make trade-off with chances of failure, decrease in efficiency and/or increase in cost. Moreover, [16] may inject unbalance current to the grid in case of non-uniform shading due to mov- ing clouds (which is very natural as such plants encompass large area). Active power filter or compensation network [19] will be required to overcome this limitation. Inverters in [12]–[16] ex- ploit PV modules to replace additional sources. However, this is at the cost of increased cable length. Maintaining MPPT from all sources may not be possible or expensive.

The above issues will not be present in the cascaded mul- tilevel inverter architecture proposed in [17]. All three phases share a common dc-bus. However, this architecture needs to transfer power through multiple isolated transformer links. This will introduce additional core-loss and will require higher im- plementation cost due to multiple smaller transformer links. All power semiconductor switches in [17] need to be rated corre- sponding to dc-bus/PV array voltage.

Cascaded multilevel inverter with floating dc-link in auxiliary bridge is proposed in [18] for PV applications. This topology will not have the problems observed in [12]–[17]. However, many of these topologies (including [18]) cannot work withouthigh frequency switching of power semiconductors.

Use of modular multilevel converter (MMC) for PV appli- cations is reported in [20], [21]. It is important to note that, the advantages of MMC (as found in HVDC application) will not be valid for PV, as too many devices with a limited dc-bus voltage of 600–1000 volts will considerably increase the con- duction loss and reduce efficiency. If the number of devices is limited, high frequency switching will not be possible to avoid. In a different attempt, efficiency and redundancy are improved by using multiple smaller inverters connected to same dc bus in [22].

High resolution asymmetrical inverter topology as observed in [23] could be a viable solution to address these issues. How- ever, high frequency link involves devices to switch at higher frequency incurring more loss and less reliability. This work aims to develop high resolution multi level inverter for solar PV applications with less number of isolated (main and auxiliary) sources with reduced power rating of auxiliary sources. The con- cept of asymmetry [23] in combination with the level doubling principle [24], [25] is exploited to boost the voltage levels.

The work is reported in eight sections. Section I deals with the important issues of a PV inverter and also critically reviewssome important PV inverter topologies reported in literature. Section II briefly explains the principle of level doubling net- work (LDN). LDN helps to improve voltage quality by creating more number of levels. Section III introduces the topology. The principle behind the selection of the nominal

14:7:2:1 ratiois explained. Section IV deals with the modulation techniqueto control such converters. A modified form of asymmetrical hexagonal decomposition is used. Implementation of vari-

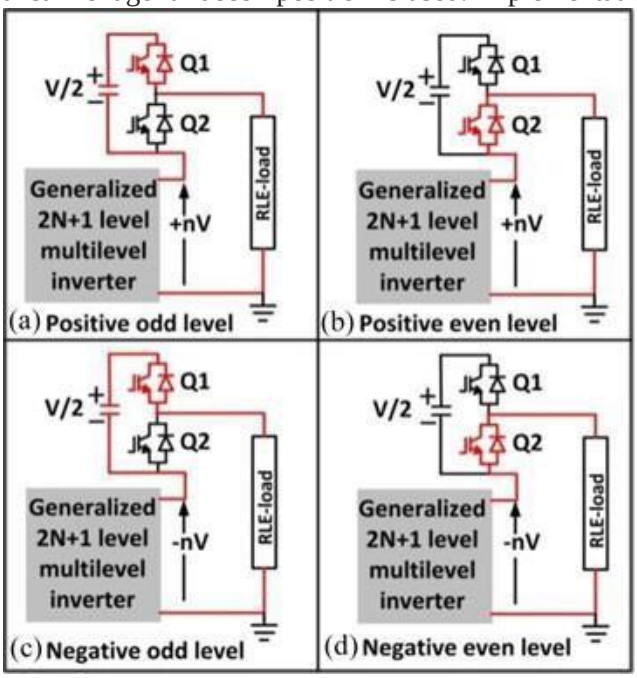

Fig. 1. Operating modes of MLI along with LDN. (a) Positive odd voltage level generated by adding the LDN voltage. (b) Positive even voltage level generated by bypassing the LDN. (c) Negative odd voltage level generated by algebraically summing the positive LDN voltage with negative voltage with respect to ground. (d) Negative even voltage level generated by bypassing the LDN.

able/fractional ratio of asymmetry is also highlighted. Section V and VI report simulation and experimental results respectively. A 9.4 kWp PV installation is connected to the grid through the proposed power converter in the laboratory. Section VII provides a brief discussion on losses and the effect of dead-time of switching devices. Section VIII concludes the work.

LEVEL DOUBLING NETWORK: BASIC CONCEPT

As discussed in Section I, proposed topology involves a level doubling network (LDN) and a full bridge inverter to form a building block. Before we proceed further, this section outlines briefly the operating principle of LDN.

Single phase version of LDN is shown in Fig. 1 along with its operating modes. The LDN is realized by adding an extra half bridge with rest of the multilevel inverter (MLI) circuit as illustrated in Fig. 1. The dc bus voltage of this LDN is half of other bridges. Fig. 1 shows that the LDN gets connected in series only when an odd level is required (in either half cycle). The network is bypassed when an even level is on demand.

Note that the charge absorbed/delivered by the capacitor in the level doubling network during a positive half cycle is same as charge delivered/absorbed during negative half cycle in the steady state.

In Fig. 1, it is assumed that, the rest of the MLI circuit can generate 2N + 1 levels (i.e. -NV to NV in steps of V) of output voltage without the use of LDN. When the half bridge (LDN) comes in operation, we get N additional levels in the positive half cycle with corresponding output voltage levels, such as: V/2, 3 V/2, 5 V/2...(2N–1)V/2 (by adding the LDN voltage with 0, V, 2 V ... (N-1)V).

On the hand, in the following half cycle also N additional levels are obtained (i.e. V/2, 3 V/2, 5

V/2… –
(2N – 1)V/2)by algebraically summing the half bridge volt-
age with V, 2 V, 3 V . . . -NV respectively. The energy spent by LDN during its positive half cycle is gained during negativehalf cycle from the rest of the network.

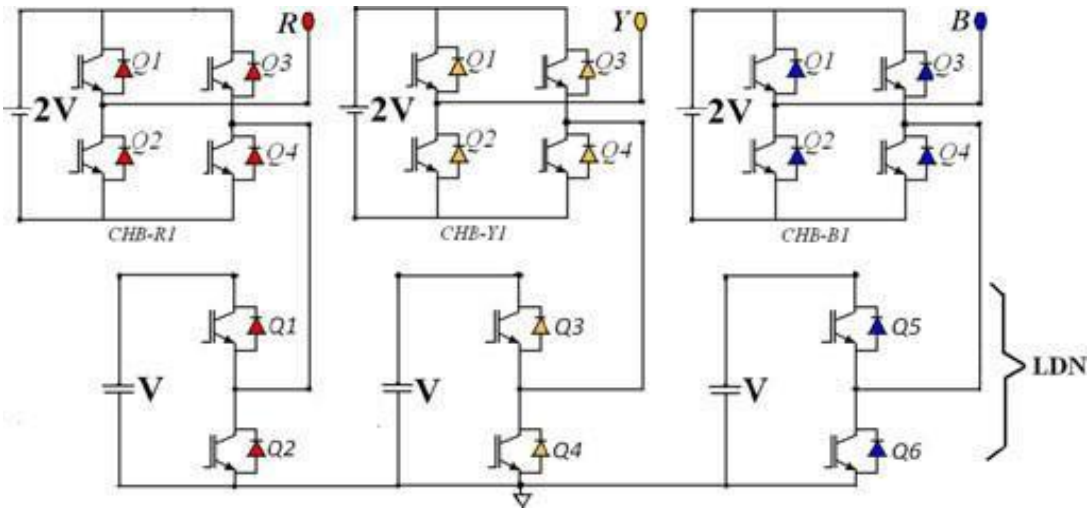

Fig. 2. A basic topological building-block.

the nature of current waveform as long as half wave symmetry is maintained. Therefore, the dc bus voltage of the LDN remains unchanged.
Due to various possible transients and disturbances, the dc bus voltage of the LDN can be higher or lower than the desired voltage for short duration. The network is having capability to adjust its voltage to desired value without closed loop control. So, the LDN does not require any additional power source. When voltage across the LDN is more than the desired voltage, its dc bus will have more discharging and when it is less, it will have more charging. Details of LDN are available in [24].

I. PROPOSED TOPOLOGY

The proposed topology has two similar topological building blocks (i.e. converter modules) at different voltage levels to achieve higher resolution/levels at the output voltage. Converter building-blocks formed by high voltage cells share most of the fundamental component of the ac output voltage. Therefore, this is termed as the main module. While the building-block formed by low voltage cells (i.e. low voltage modules or auxiliary mod- ules) are responsible to maintain power quality without signif- icantly compromising with switching and conduction losses. These modules are formed by a full bridge and a half bridge per phase as shown in Fig. 2. As the half bridges operate as LDN, the corresponding dc-bus capacitors maintain a voltage equivalent to half of the full bridges [24]. Full-bridges in main and auxil- iary modules are called main-bridge (MB) and auxiliary-bridge (AB) respectively. Similarly, LDNs in main and auxiliary mod- ules are called main-LDN (MLDN) and auxiliary-LDN (ALDN) respectively.
Space-vectors possible to obtain from any of the topological building blocks shown in Fig. 2 are illustrated in Fig. 3. To maintain simplicity of the figure, arrows are replaced by dots at the location of arrow-heads as shown in right-side of the figure. Space-vectors indicated by large and smaller dots are obtained by the full bridge at a dc bus voltage 2 V, and LDN with dc-bus voltage V respectively. It may be noted that, the space-vector domain presented in Fig. 3 is corresponding to a five-level inverter formed by the topological building block in Fig. 2. Voltage ratio between main and auxiliary building- blocks should be maximized in order to have highest resolution in output voltage and minimize the power handled by auxiliary building-block. Resolution should be high enough with limited

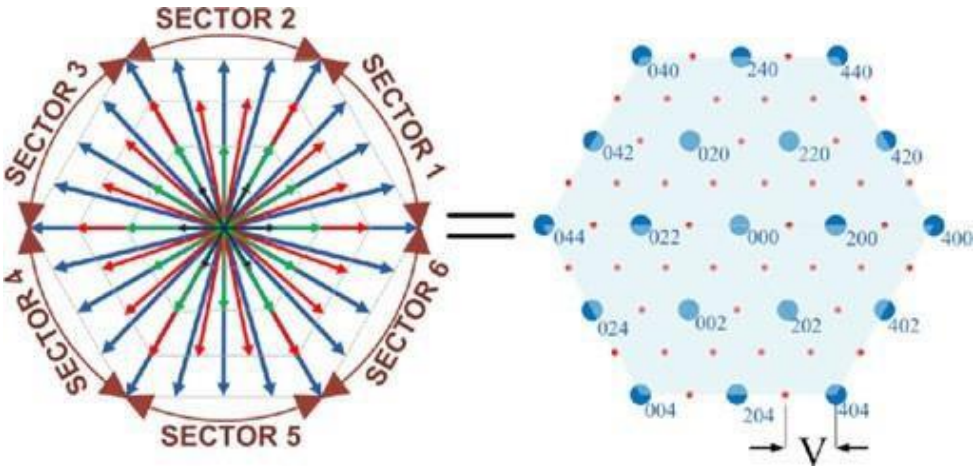

Fig. 3. Space-vectors obtained by the topological building block shown in Fig. 2.

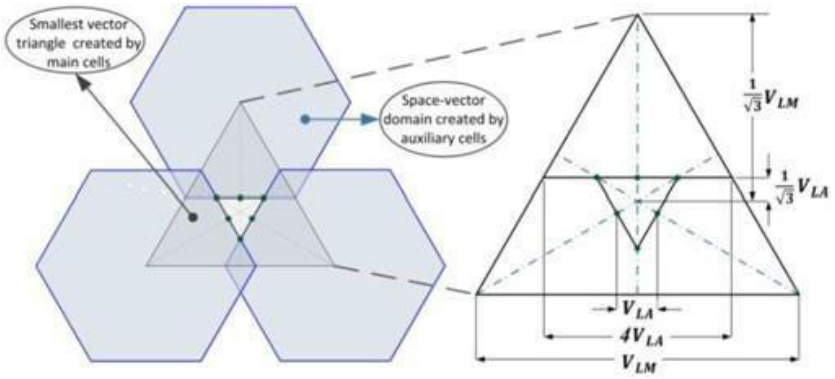

Fig. 4. Space-vector domains generated by auxiliary cells associated with the smallest vector-triangle of space-vector plane.

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component in the output voltage at any operating condition. This calls for equal distance between all the adjacent space-vectors inside the resultant space-vector plane created by main-subsection and auxiliary-subsection together. This is the basis of finding the voltage ratio between MB and AB (or MLDN and ALDN) as shown in Fig. 4. If V is the voltage of ALDN, then any point inside the space-vector domain created by auxiliary-building-block will have nearest space-vector at adistance less than or equal to (1/{3)VLA as shown in Fig. 4. Where, VLA is the auxiliary LDN voltage. So, the maximum error between nearest space-vector and the reference space- vector at any given instant will be (1/ √ . Three space- vector domains of auxiliary-subsection are drawn by centering them on three corners of the smallest vector-triangle formed by the space-vector plane of main-subsection as shown in Fig. 4. So, one side of the smallest vector triangle formed by main subsection is equal to dc-bus voltage VLM of MLDN at steady- state as shown in Fig. 4. Based on the vector diagram illustrated in Fig. 4, relation between VLM and VLA can be formed as given in (1). So, the maximum voltage of MLDN can be 7 times higher than the ALDN in order to limit the difference between reference vector and its nearest space-vector to (1/√ as obtained in (2).

$3V_{LA}$
$3V_{LA}$

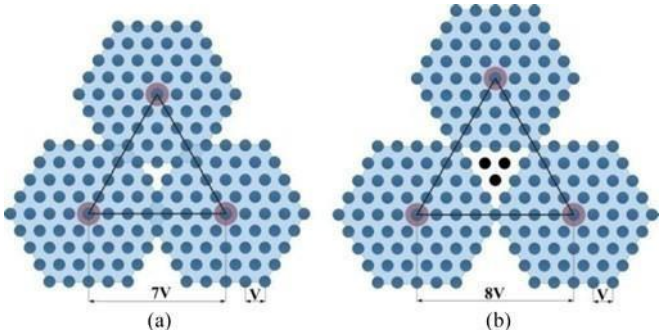

Fig. 5. Space-vectors domains of auxiliary-subsection are placed on the cor- ners of equilateral vector-triangle formed by LDN voltage of next topological sub-section. (a) Ratio of LDN voltages 1:7 (b) Ratio of LDN voltages 1:8.

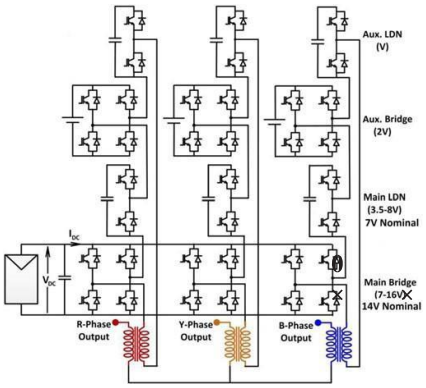

Fig. 6. Complete circuit diagram of the proposed topology for PV central inverters.

This is an effective way to increase line voltage resolution. Large number of achievable space-vectors ensures that stair-case mod- ulation will be sufficient to inject high-quality current waveform to the grid. This will help to minimize switching losses. Lowest voltage cells may observe relatively higher frequency switching. The dc-bus voltage of the lowest voltage cells will be at (1/14)th time less than the PV array operating voltage. So, lowest volt- age cells (that operates at a frequency 0.9–2.4 kHz depending on operating condition) will not have dc-bus voltage greater than 1000/14 ≈ 72 V. Power MOSFETs will be

a good choice for such dc-bus voltage, as ON-resistance is significantly low for power MOSFET rated below 100 V of blocking voltage (ON resistance of power MOSFET exponentially drops with the de- crease in blocking-voltage).
Depending on insolation and operating conditions, main
bridge voltage *V HM* is allowed to vary in the range 7 V to 16 V. This range is sufficient to operate the PV inverter under all practical operating conditions (considering variation in inso- lation and temperature). The dc links of the main bridges may be merged (exploiting the isolation provide by the transformers) to optimize the size of dc link capacitor. It is important to note that same numbers of switches are used as observed in [23], i.e. twelve switches per phase, but the maximum number of levels in [23] can be 53, while the proposed topology can achieve a maximum of 65 levels in line-to-line voltage. At the same time total number of isolated sources required in [23] are 6, while only 3 isolated sources are required for the proposed topology. These isolated sources may be optimized using the redundancy to achieve a given space vector.

MODULATION STRATEGY (FRACTIONAL ASYMMETRY)

Modulation strategy is developed for satisfactory operation of LDNs at all conditions of the PV inverter, and ensure staircase modulation throughout the operating range without dc-offset in phase voltage to avoid core-saturation of open winding trans- former.
Proposed high resolution multilevel inverter will result in 3097 possible space-vectors as indicated in Fig. 7. Large num- ber of space-vectors provides flexibility to reach closest point of a reference vector. However, this also creates challenging situa- tion to identify the closest space-vector in shortest possible time and with minimal computational resources. Hexagonal decom- position [26] is modified to satisfy the operation of LDNs. This is assured by ensuring that a given phase voltage is achieved by combination of cell voltages given in Table I only.
Power-voltage characteristics of a typical PV cell at differ- ent operating conditions are shown in Fig. 8. It is clear that, maximum power point voltage V MPP is a stronger function of temperature than insolation. Fig. 8 also indicates that, it will be good enough to vary the modulation index from 0.5 (at rated power) to unity (at lower power range).
As a common practice in dc-dc converter-less PV inverters, it is ensured that inverter will be able to synchronize with the grid up to a minimum voltage corresponding to solar insolation of 0.1 Sun operating at maximum ambient temperature.

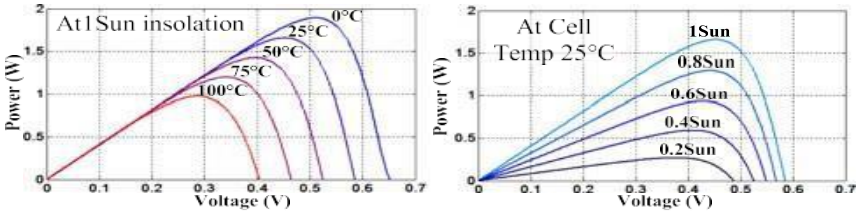

Fig. 8. Typical V-I characteristics of a PV cell and its dependency on (a) temperature (b) insolation.

is ensured by setting the rated open-circuit dc-bus (PV-array) voltage high (almost double the requirement) to synchronize with the grid. As the insolation is reduced from its maximum value, dc-bus voltage of the main bridges and main LDNs will reduce and modulation index will be controlled to feed power to the grid.
Space-vector plane will therefore shrink as a result of re- duction of dc-bus voltages of main building-block. This phe- nomenon is illustrated in Fig. 9. Locus of the reference vector required to synchronize with balanced three-phase ideal voltage is shown by a circle. Ignoring minor change in grid voltage, the radius of this circle is assumed to remain constant.

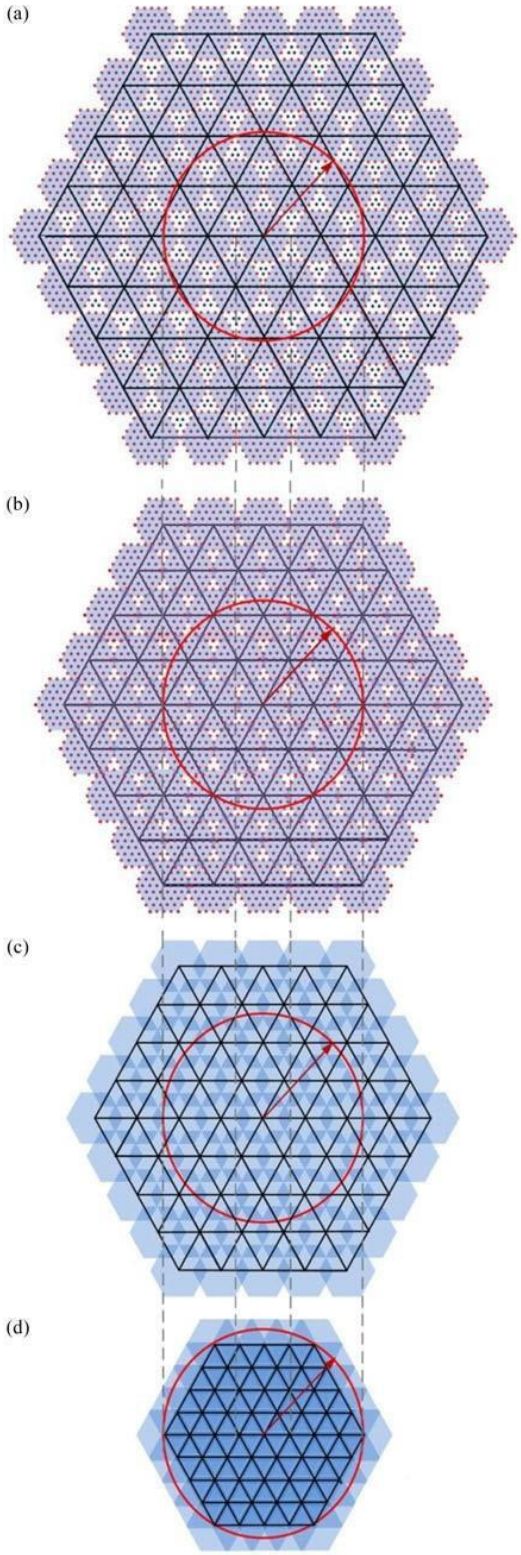

Fig. 9. Shrinkage of space vector plane with reducing solar insolation: Main bridge: Main LDN: Auxiliary bridge: Auxiliary LDN voltage ratio are given by (a) 16:8:2:1 at open circuit voltage and full insolation (b) 14:7:2:1 at MPP andfull insolation (c) 12:6:2:1 (d) 7:3.5:2:1.

TABLE II SIMULATION PARAMETERS

Parameters	Value
MPP voltage @ 1sun and 25 °C	140 V
Range of operating voltage	75–160 V
Main bridge voltage range	75–160 V
Main LDN voltage range	37.5–80 V
Auxiliary bridge voltage	20V ± 5%
Auxiliary LDN voltage	10V ± 5%
RMS grid voltage line to line (3-Φ)	110 V

SIMULATION RESULTS

Simulation results are obtained using MATLAB/Simulink. Note that such configuration is suitable for central inverters (typically above 100 kW power rating). DC-bus voltage of such inverter varies in the range of 600 V–900 V. Upper limit of dc- bus voltage is bounded by terminal-to-frame insulation limit of PV module (usually 1000 V). In this investigation a down-scale version is considered for both simulation and experimentation to confirm the usefulness of the concept proposed. Major sim- ulation parameters are listed in Table II. Line-to-line voltages, phase-voltages and different cell voltages are plotted for dif- ferent input voltages (within the range of PV array voltage) to understand the nature of the waveforms and the harmonic con- tents in the phase voltage. It will be possible to understand the nature of LDN voltage and its self-balancing characteristics.

Asymmetrical hexagonal decomposition is used to select the specific space vectors. Availability of large number of space vectors helps to select the right combination matching the space vectors for first half and second half of the waveforms such that no dc components are generated in the phase voltage wave- form. Thus any problems related to transformer saturation may be easily avoided. Fig. 10 illustrates phase-voltage and corre- sponding cell-voltages (Main H-bridge VHM , main LDN VLM , auxiliary bridge VHA and VLA) at different operating conditions corresponding to Fig. 9.

Waveforms of VLM and VLA in all cases are repetitive after a half cycle. This confirms that the LDNs will not consume any

power over a complete cycle, as it contains only dc-components and even harmonics. Fig. 11 shows line-to line voltage VBR at different operating conditions considered in Fig. 9.

This is achieved by adjusting the phase-voltages VB and VR through modulation technique as shown in these figures. THD of line-to-line voltage was limited below 1.7% in all line-to-line voltage waveforms illustrated in Fig. 11.

Switching frequency of main-bridge (f HM), main-LDN (f_{LM}), auxiliary-bridge (fHA) and auxiliary-LDN (fLA) are plot- ted in Fig. 12. It is observed that, the auxiliary-LDN switches at a frequency range 0.9 kHz–2.4 kHz at a voltage less than

or equal to (1/14)th of rated PV array dc-bus voltage. Such a low operating voltage at a moderate switching frequency makes MOSFETs ideally suitable for this module. Low on-state drop and low switching loss of the MOSFETs will improve the performance of the converter. Whereas, for the main module is observed to operate up to a maximum frequency of 150 Hz.

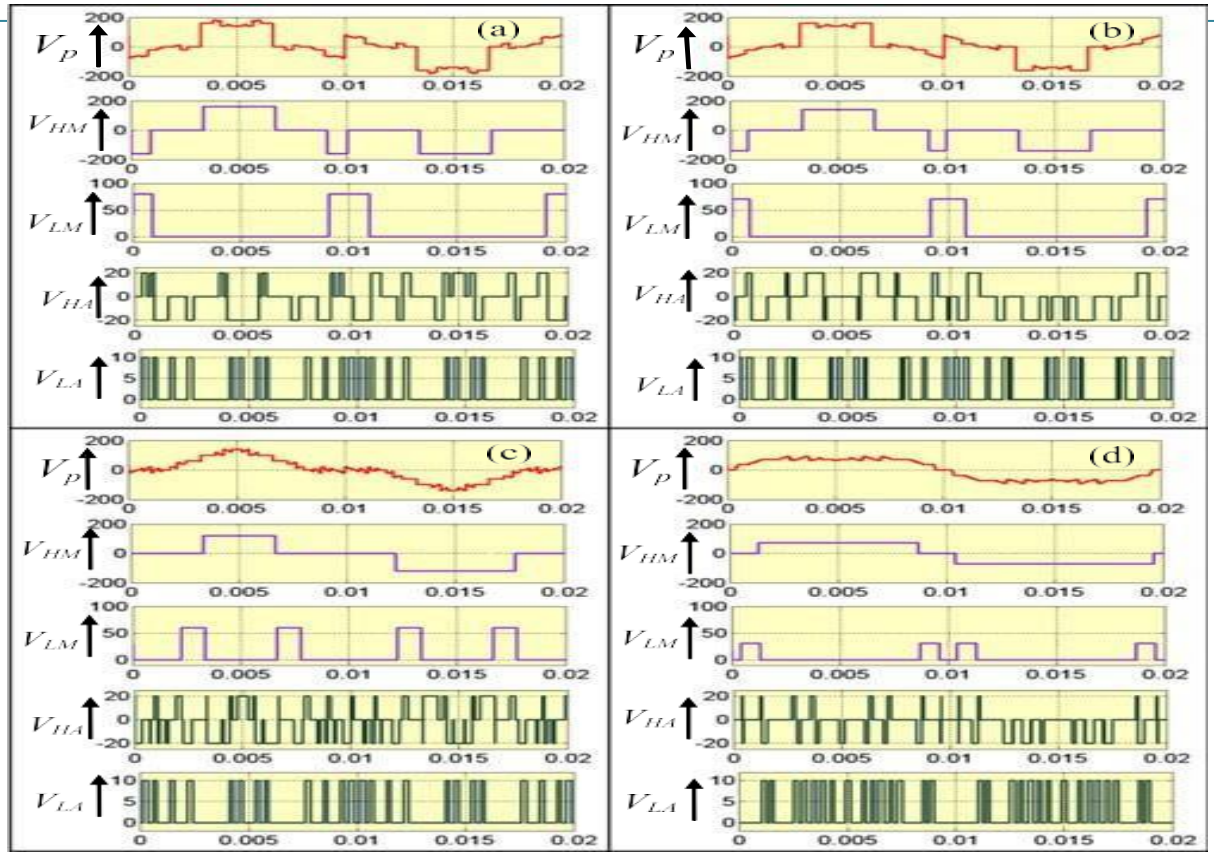

Fig. 10. Phase voltage without dc-components and corresponding cell volt- ages at different main-bridge voltage to synchronize with grid voltage: Main bridge: Main LDN: Auxiliary bridge: Auxiliary LDN voltage ratio are given by (a) 16:8:2:1 (b) 14:7:2:1 (c) 12:6:2:1 and (d) 7:3.5:2:1 (ALL X AXES ARE TIME IN SECONDS

CONCLUSION

This paper introduces a novel asymmetrical multi-level inverter with a nominal voltage ratio of 14:7:2:1. The configuration leverages the benefits of a level-doubling network, where one full-bridge inverter and a level-doubling network constitute a topological building-block. By combining two such building-blocks with a nominal asymmetry ratio of 7:1, the paper achieves the 14:7:2:1 configuration for the 3-phase version of the converter. The applicability of the converter for solar photovoltaic (PV) applications is emphasized.

The study demonstrates that the converter effectively evacuates power from solar arrays, even under extreme variations in insolation and temperature, by utilizing variable and fractional asymmetry. Throughout the operating range, the total harmonic distortion (THD) of the output voltage waveform remains within 1.7%. Under nominal conditions, the main module handles about 99% of the power, with the LV (Low Voltage) module managing the remaining 1%. The distribution of power is plotted for different operating voltages, with the worst-case scenario showing corresponding power distributions of 90.5% and 9.5%, respectively. This flexibility allows for the selection of different power electronic devices to optimize converter performance.

To assess performance across varying asymmetry ratios, the proposed converter is simulated using MATLAB/Simulink. Additionally, an experimental setup is fabricated in the laboratory, utilizing a 9.4 kWp rooftop solar PV installation. Both simulation and experimental results confirm the effectiveness of the proposed converter for solar PV applications.

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