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## DESIGN AND IMPLEMENTATION OF MUX BASED BARREL SHIFTER ON SPARTAN 6

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Abstract:Shifters are commonly used in computer intensive applications such as digital signal processing, floating point arithmetic for shift and rotate operations. The shift and rotate instructions shift the data by one bit in one machine cycle. The number of shifts equal to number of machine cycles. This drawback can be overcome by mux based barrel shifter. The barrel shifter takes n-bits of data input and gives n- bits of data output depends on the control bits such Dir, Shift\_amt, Shift/rotate. The proposed design examines the techniques for detecting the results that overflow and zero in parallel with shift and rotate operations.

Keywords Barrel shifter, mux, shift\_amt, dir.

#### 1. INTRODUCTION

Shift is an operation done on all the bits of input data in which they are moved by a determined number of places either to left or right. The shift operation is performed by shifter, which requires a clock cycle for each bit of shift. The proposed mux based barrel shifter works to shift the data by incremental stages which avoids extra clocks and reduces the time spent in shifting/ rotating the data.

A Barrel Shifter is a digital circuit that can shift or rotate a data by specified number of bits in single clock cycle. The Barrel Shifter is commonly used in computer intensive application such as DSP, General purpose Microprocessor in implementation of floating point arithmetic [5].

There are two common architectural layouts array shifter and logarithmic shifter. An array shifter decodes the shift amount into individual shift bit lines that mesh across all input data values at each crossing point, the gate will either allow or not allow the input data value to pass the output line, controlled by a shift bit line. The disadvantages of this architecture are requirement of decoder and each input data line, sees a load from every shift bit line. In logarithmic shifter, shifter is divided into log2N stages where N is the input data length [4]. The proposed mux based barrel shifter belongs to the logarithmic shifter architecture and performs rotate, logical shift and arithmetic shift along with detection of overflow and zero flag [1]. The mux based barrel shifter overcomes the disadvantages of array shift architecture.

## 2. DESIGN OVERVIEW

In the proposed design, barrel shifter implemented as a sequence of multiplexors. In this design output of one mux is connected to the input of next mux in a way that depends on the shift distance (shift\_amt). The number of multiplexors required are  $N(\log 2(N))$ , for a N-bit data.[4] Barrel Shifter is designed using mux and then realized the functionality. It is coded in verilog using Xilinx 13.1 ISE simulator.

The mux based barrel shifter can perform rotate, logical shift and arithmetic shift in both left and right direction along with detection of zero and overflow flag. The "Table 1" shows the operations performed by the barrel shifter.



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#### Table 1. Barrel shifter functionality table

Dir	Shift	Rotate	Mode of operation
0	0	0	Logical right shift
0	0	1	Rotate Right
0	1	0	Arithmetic right shift
1	0	0	Logical left
1	0	1	Left rotate
1	1	0	Arithmetic Shift Left

Fig.1 is the block diagram of mux based barrel shifter, as the name reveals this design primarily utilizes multiplexors and data reversal mechanism to carry out its operation. The shifter / rotator is a single directional shifter. To operate it in bidirection, data reversal is used before and after the shifter / rotator stage. The control signal "dir" specifies the direction of data shift. Barrel shifter basically offers 6 operations such as rotate right, rotate left, arithmetic right shift, arithmetic shift left, logical right shift, logical left shift.

Rotation is similar to shifting, in that it moves bits to the left. With rotation however bits which "fall off" the left side get tacked back on the right side as lower order bits. While in shifting the empty space in the lower order bits after shifting is filled with zeros.

Rotate operation is a cyclic shift either to left or right, depending on the rotate amount. Logical right shift is similar to rotate right operation but here lower order bits are lost and higher order bits are filled with zeros, depending on shift amount.



Fig 1: Block diagram of mux based barrel shifter

In logical left shift operation, higher order bits are removed, remaining bits are shift from lower order to higher order position and lower order bits are filled with zeros. The arithmetic right shift operation is similar to logical right shift operation except higher order is replicated in higher order bits depends on the shift amount. The arithmetic right shift operation maintains sign of data. Arithmetic left shift operation is combination of arithmetic right shift and logical left shift operations. In arithmetic left shift operation, bits shift from lower order bits to higher order bits are filled with zeros depends on shift amount. It also retains sign bits.

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A zero flag is a simple 1-bit flag that indicates whether the result is zero. The flag is useful when the result is used in an equality test with zero. The overflow flag is computed in a series of steps corresponding to the break down within the shifter / rotator. Each step uses number of multiplexors, during shift, these multiplexors selects those bits that pass beyond or on to the data sign bit, which during shift left operation inhabits the LSB position of the input to the shifter / rotator [1].

The proposed mux based barrel shifter is designed to detect the zero and overflow conditions in parallel with shift and rotate operations.

## 3. SIMULATION RESULTS

The mux based barrel shifter is synthesized and simulated using xilinx13.1ISE simulator. Fig.2 to Fig.7 shows simulation results of rotate right, rotate left, logical right shift, logical left shift, arithmetic right shift, arithmetic left shift operations respectively. The device utilization summary is shown in Fig.8, which indicates area consumed by the design is less.

Name	Yalue	p,400 rs p,500 rs p,500 rs p	2,700 ns
<ul> <li>Data_n(7:0)</li> </ul>	11110000	11110	a)
a ata	ņ		
1 50	2		
a rotate	1		
ieft .	p		
b[2:0]	011	to1	
Um ov	0		
1.	Ú		
Dista_nut[7:0]	00011110	000111	10

Fig. 2 Simulation result of rotate right operation.

Name	Value			1,600	ns	1,700 ns	
🕨 📑 Data_in[7:0]	11110	11110000				111	10000
1 sra	0						
1 sla	o						
🗓 rotate	1						
14 left	1						
🕨 🐳 b[2:0]	011					0	11
un ov	0						
l <mark>a</mark> z	o						
▶ 📲 Data_out[7:0]	10000	111				100	D0111
Fig. 3	3 Simulat	ion res	ult of ro	otate lef	t operat	ion.	
Name	Value	100 ne	i na sel	500 ns	1600 n	farm.	700 ns
Data_in[7:0]	11110000					11110	000
a 978	0						
1 sta	0						
inotate	0						
1 left	0						
b[2:0]	411					11	t -
10 mil							

Fig. 4 Simulation result of l	ogical right s	hift operation
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Device Utilization Summary (estimated values)					
Logic Utilization	Used	Available	Utilization		
Number of Slice LUTs	38	2400		1%	
Number of fully used LUT-FF pairs	0	38		0%	
Number of bonded IOBs	25	102		24%	

Fig.8 Device utilization summary. CONCLUSION 0000000



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This paper has examined mux based data reversal barrel shifter. The design is synthesized and simulated using Xilinx 13.1 ISE simulator. It estimates the less delay along with the detection of zero and overflow flag.

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