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High Step-Up DC-DC Converter without Isolation and Low Switch Voltage Stress

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ABSTRACT
A novel high step-up DC-DC converter topology is introduced here, fusing a conventional inductor-based Buck cell with a charge pump mechanism. When compared to a traditional Boost converter made for the same voltage gain, its primary benefits are the lowest switch voltage stress determined by the input voltage and less energy in the magnetic element. The suggested topology is obtained by modifying the standard voltage-doublers charge pump cell, which enables the fidelity capacitor voltages to be dependent on the switch duty-cycle because of a connected inductor. The intrinsic leakage inductance of the connected inductor benefits the capacitor charging and discharging channels equally, resulting in soft diode turn off without reverse recovery issues and ringing free operation. An appropriate Buck inductance design enables quasi-square wave operation, enabling the switches to be turned on at zero voltage. Appropriate design parameters are suggested in order to get the intended mode of operation for the converter without requiring an iterative procedure. Theoretical analysis and expectations are supported by experimental results based on a 44V to 400V - 300W prototype, which display a very flat efficiency curve that remains above 90% down to a tenth of the nominal power.
KEYWORDS: ***DC-DC converter 1, Boost converter 2, step-up DC-DC converter 3, switch voltage stress 4, step-up DC-DC converter***

1. INTRODUCTION

The world is greatly affected by the severe environmental pollution caused by the use of fossil fuels including gas, coal, and oil. The supply of fossil fuels and the demand for energy worldwide are in stark contrast to one another. The two main things preventing human advancement have been the scarcity of energy and environmental pollution. Finding sustainable energy sources is becoming more and more important. One important component of the global energy mix is renewable energy, which will also contribute significantly to the production of electricity. High step-up dc/dc converters are commonly used in many renewable energy applications, such as fuel cells, wind power, and solar systems, because renewable energy systems produce low voltage output.

Unfortunately, the output voltages of the renewable systems are relatively low. In order to satisfy the high bus voltage requirements for the full-bridge, half-bridge, or multilevel grid inverters, the sources has to be connected to series in order to bring out a grater voltage ratio , which again suffers from the voltage mismatches and the module level mismatch issues .

The boost switch experiences substantial current stress due to large duty cycles. The resistances of the components or leakage inductance should theoretically prevent conventional step-up converters like the boost converter and fly back converter from achieving a high step-up conversion with high efficiency. Furthermore, a higher duty cycle would be needed for the converters in order to increase the voltage boost. The boost switch experiences substantial current stress due to large duty cycles. Because they provide energy in a clean manner, renewable energy technologies are employed extensively.

Unfortunately, a high voltage ratio in comparison to the grid cannot be provided by

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renewable energy sources. A high gain dc-dc converter is needed to connect the renewable generators to the grid. It takes up a lot of room and money to implement such dc-dc converters.

1. CONVERTER TOPOLOGIES

A. Conventional Boost converter

A converter with a high step-up gain ratio and high efficiency is more crucial to meeting grid standards. Large switch duty ratios are necessary for traditional boost and buck-boost converters to obtain substantial voltage gains. The resistances of the components or leakage inductance should theoretically prevent conventional step-up converters like the boost converter and fly back converter from achieving a high step-up conversion with high efficiency. Furthermore, a higher duty cycle would be needed for the converters in order to increase the voltage boost. We offer a high step-up DC-DC converter topology that combines a conventional inductor-based Buck cell with a charge pump mechanism.

A modification of the standard voltage-doublers charge pump cell yields the suggested topology. To make the flying capacitor voltages dependent on the switch duty-cycle, a linked inductor is employed. Due to the coupled inductor's inherent leakage inductance, both the charging and discharging channels for capacitors benefit from soft diode turn off that occurs without reverse recovery issues or ringing

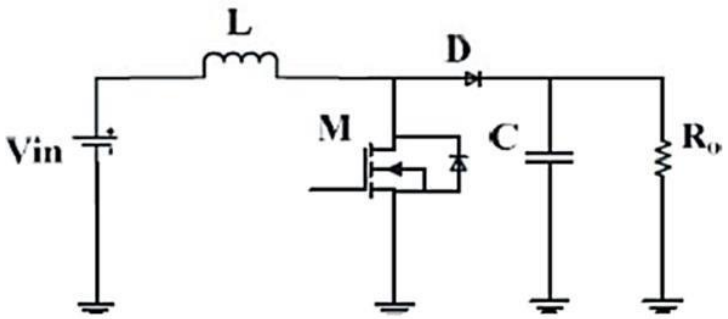

Fig1. Classical boost converter

The parasitic resistive components in the circuit limit the greatest voltage gain that can be obtained, and at higher duty ratios, efficiency is significantly decreased. The diode conducts for a brief time, which causes diode reverse recovery issues. Larger ripples on the high output voltage and input current would also worsen the converter's efficiency.

To obtain high voltage conversion ratios, linked inductors or high frequency transformers are typically utilized. Increasing the number of winding turns required for larger gains necessitates more complex transformer design and higher leakage inductances. Voltage clamping techniques are necessary to limit voltage strains on the switches as a result of voltage spikes across the switches. As such, it adds complexity to the design.

In theory, high step-up conversions with high efficiency are impossible for traditional step-up converters like the boost converter and fly back converter. Furthermore, high-power applications cannot employ typical step-up converters with a single switch due to element resistances or leakage inductance, which increases conduction losses when there, is a strong current ripple in the input.

Conventional step-up converters lack the necessary elements' resistances or leakage inductance to achieve high gains. Additionally, because of their high voltage stresses and large input current ripple, which increases conduction losses, these converters are not suitable for heavy load operation. A novel range of high voltage gain dc-dc power electronic converters has been launched,

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with the aim of achieving elevated voltage conversion ratios.

A traditional interleaved boost converter is a good option for high step-up and high power applications. The converter's structure can be changed to enable it to function in the high gain conversion state. For high-power applications and power factor correction, the traditional interleaved boost converter is a great option.

The voltage strains on semiconductor components are identical to the output voltage, which is unfortunate given the restricted step-up gain. Therefore, it makes sense to alter a traditional interleaved boost converter for high step-up and high-power applications in light of the previously described concerns. The combination of a conventional inductor-based Buck cell with a charge pump mechanism is described as a high step-up DC-DC converter topology.

A modification of the standard voltage-doublers charge pump cell yields the suggested topology. To make the flying capacitor voltages dependent on the switch duty-cycle, a linked inductor is employed. The linked inductor's intrinsic leakage inductance benefits the capacitor charging and discharging channels equally, resulting in soft diode turn off without reverse recovery issues and ring-free operation.

B. Modified fly back converter

Many interleaved structures and some asymmetrical interleaved structures have been discovered to be useful for boosting the voltage gain ratio in the numerous modifications that have been done to the traditional converters to suggest for high gain converter design. One easy way to achieve a high step-up gain is to modify the boost-fly back converter, as illustrated in Fig. A connected inductor is used to realize this gain. Since the converter operates similarly to an active-clamped fly back converter, the leakage energy is recovered and sent to the output terminal. Figure 2 depicts an interleaved boost converter with a voltage-lift capacitor and a voltage multiplier module to raise the voltage level.

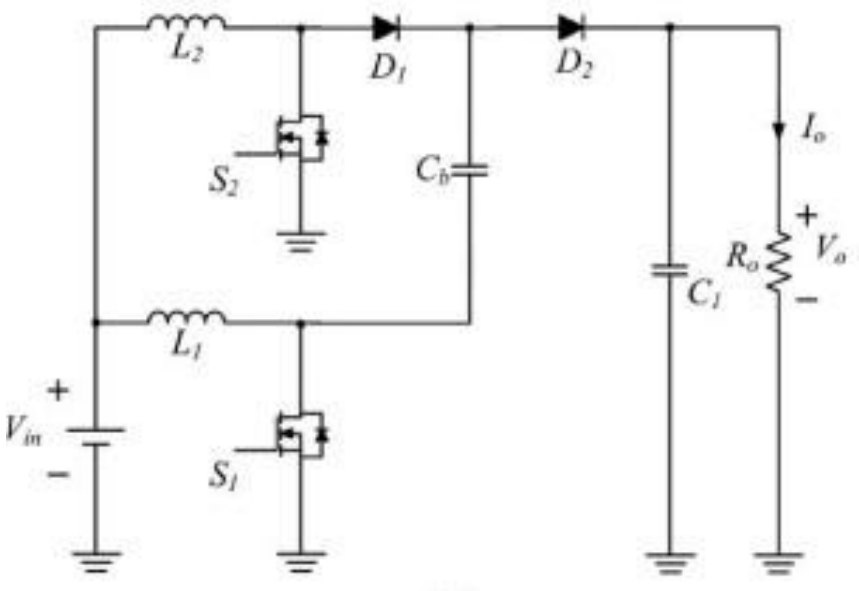

Fig 2 Voltage lifting scheme with a modified converter

This method lowers input current ripple and achieves extra voltage gain through the voltage-lift capacitor, making it suited for power factor correction (PFC) and high-power applications. It is quite similar to the standard interleaved type, but with an added voltage lifting methodology.

Afterwards, a proposal for an asymmetrical interleaved high step-up converter is made, which integrates the benefits of the two converters discussed earlier. It includes a minimum

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duty ratio control, voltage lifting, and step-up gain.

C. Inter leaved converter with voltage multiplier module

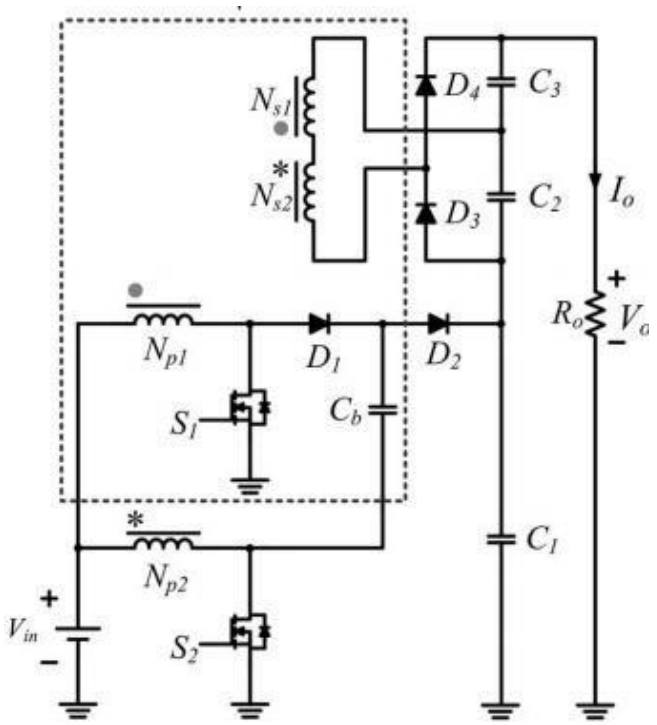

Fig 3 Interleaved boost converter with a high step-up conversion and a voltage multiplier module.

Fig. 3 illustrates the high step-up interleaved converter with a voltage multiplier module. The voltage multiplier module creates a modified boost–fly back–forward interleaved structure by inserting it between a regular interleaved boost converters. It is made up of two coupled inductors and two switching capacitors. The phase whose switch is in the OFF state acts as a fly back converter, while the other phase whose switch is in the ON state acts as a forward converter when the switches turn off one after the other.

The secondary windings of the linked inductors with Ns turns are connected in series to increase voltage gain, and the primary windings of the coupled inductors with Np turns are used to reduce input current ripple. The connected inductors have identical turn ratios. Continuous conduction mode (CCM) is used by the converter, and steady state power switching duty cycles

Later, a voltage multiplier module made up of coupled inductors and switching capacitors was merged with a converter based on the traditional interleaved boost converter. Additional voltage conversion ratio is provided by the switching capacitors, and the connected inductors can be engineered to increase step-up gain. Furthermore, the energy stored in the magnetizing inductor will transfer via three different paths when one of the switches turns off. As a result, the current distribution reduces diode reverse recovery losses in addition to lowering conduction losses by lowering effective current through some diodes.

D. High step up inter leaving boost converter

The voltage multiplier module and high step-up interleaved converter are depicted in Fig. 1.5. Created by inserting the voltage multiplier module between a standard interleaved boost converter and two connected inductors and switching capacitors, the result is a modified boost–fly back–forward interleaved construction.

The phase whose switch is in the OFF state acts as a fly back converter, while the other phase whose switch is in the ON state acts as a forward converter when the switches turn off one after the

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other. The secondary windings of the linked inductors with Ns turns are connected in series to increase voltage gain, and the primary windings of the coupled inductors with Np turns are used to reduce input current ripple. The connected inductors have identical turn ratios.

Furthermore, given an input big current ripple that increases conduction losses, typical step-up converters with a single switch are inappropriate for high-power applications due to element resistances or leakage inductance.

Due to their high element resistances or leakage inductance, conventional step-up converters are not suitable for achieving high gains. Additionally, because of their high voltage stresses, these converters are not suitable for heavy load operation given large input current ripples, which increase conduction losses. A new series of high voltage gain dc-dc power electronic converters has been introduced to achieve high voltage conversion ratios.

A traditional interleaved boost converter is a good option for high step-up and high power applications. The converter's structure can be changed to enable it to function in the high gain conversion state. For high-power applications and power factor correction, the traditional interleaved boost converter is a great option.

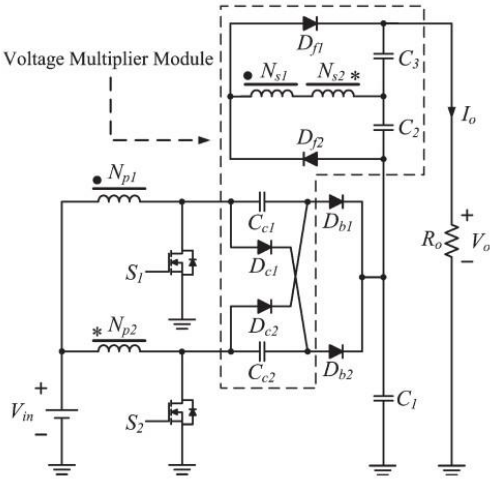

Fig 4 A modified interleaved high step up converter with a voltage multiplier module

2. TOPOLOGY DESIGN

Not only do the resonant capacitors Cr1 and Cr2 function as a component of the resonant tank.the rectifier and attached to the output voltage V negative potential

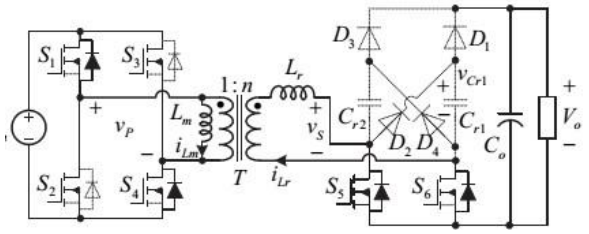

Fig 5 Topology Design

This design includes a high frequency transformer, output diodes D1 and D3, regenerative diodes D2 and D4, resonant capacitors Cr1, Cr2, and a resonant inductor Lr. The active switches S1 and S2 are used to control the output power. The resonant tankiscomposedofthreeelements,Cr1, Cr2 and Lr. Depending on the input voltage, the converter can be used in either boost or buck mode. The

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transformer's magnetizing inductance, or inductor Lm, and the transformer's secondary to primary turns ratio, or n, are expressed respectively.

Similar to a voltage multiplier, the resonant capacitors Cr1 and Cr2 are utilized to double the output voltage in addition to being a component of the resonant tank. To manage the output voltage and power, phase-shift control is used. A voltage multiplier with resonant full bridge that has isolated DC-DC conversion is designed. Lr is a resonant inductor in the circuit, whereas Cr1 and Cr2 are resonant capacitors. D2 and D4 are regenerative diodes, while D1 and D3 are output diodes. This is an isolation-related high frequency transformer. The active switches S1 through S4 are used to control the output power.S5 and S6 are attached to the output voltage Vo's negative potential and positioned on the rectifier's underside.

3. METHODOLOGY OF PROPOSED SYSTEM

A. Influence Of Non-Ideal Back-Emf On Commutation Point Detection And Optimal Commutation Control

First, the impact of non-ideal back-EMF on sensor less commutation point identification is examined. The best commutation control strategy is then suggested after comparing the electromagnetic torque variation and efficiency of the motor driven by square current at various commutation locations. In addition, an integrated nonlinear model of the motor and drive circuit with exact back-EMF characteristics is created for the low inductance motor with non-ideal back-EMF and buck converter front-end drive structure. The viability of linearizing the model is examined in light of the nonlinear model. A stable speed controller based on the linearization model is built, and the linearization method based on input-output feedback method is proposed.

B. Deviated commutation points detected by virtual neutral points method due to non-ideal back-EMF

When the neutral point voltage is not measurable, three Y-type linked resistor networks are utilized in the virtual neutral point-based position sensor-less ZCP detection method, as illustrated in Figure 6, to generate a virtual neutral voltage signal. Where s stands for the virtual neutral point, n for the three-phase windings' neutral point, and g for ground.

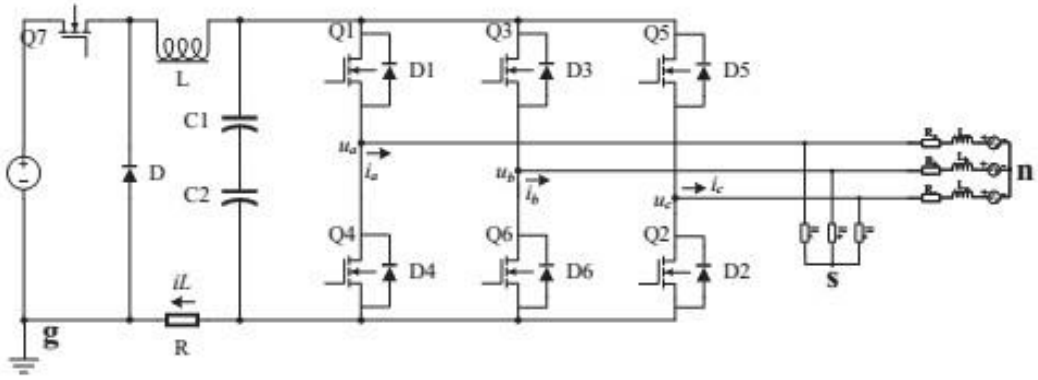

Fig 6 Schematic diagram of zero-crossing detection method based on virtual neutral point

The terminal voltage mathematic model of the BLDC motor is written as (1).

$$U_{xg} = L_x \frac{di_x}{dt} + R_x i_x + E_x + U_{ng} \quad (1)$$

where *Uxy* represents the voltage difference between *x* and *y*, *Lx*, *Rx*, *ix*, *Ex* represent the inductance, resistance, phase current and back-EMF of phase *x*, respectively. Here, the three-phase resistance and inductance are treated as constant and equal. The harmonic form expression of the three-phase non-ideal back-EMF of the BLDCM is as(2)

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$$\begin{cases} E_a = \omega_e k_e e_a(\theta_e) \\ E_b = \omega_e k_e e_b(\theta_e) \\ E_c = \omega_e k_e e_c(\theta_e) \end{cases} \quad (2)$$

$$\begin{cases} e_a(\theta_e) = \sum_{m=1}^{\infty} A_{am} \sin(m(\theta_e)) + D_a \\ e_b(\theta_e) = \sum_{m=1}^{\infty} A_{bm} \sin\left(m\left(\theta_e - \frac{2\pi}{3}\right)\right) + D_b \\ e_c(\theta_e) = \sum_{m=1}^{\infty} A_{cm} \sin\left(m\left(\theta_e + \frac{2\pi}{3}\right)\right) + D_c \end{cases}$$

Where

Ωe represents the electromagnetic speed, *ke* represents the back-EMF coefficient, *θe* represents the electrical angle position, *Axm* represents the *m*th harmonic coefficient of the *x*phase back-EMF, *Dx* represents the DC offset of the *x* phase back-EMF, and *ex* represents the *x* phase back-EMF waveform shape function. Through offline measurement, the relevant coefficients can be found. Kirchhoff's law states that another way to represent the terminal voltage is as (3).

$U_{xg} = U_{xs} + U_{sg}$……..(3)

The following constraint equations can be obtained according to the Y-type connection

$$U_{sg} = \frac{1}{3}(U_{ag} + U_{bg} + U_{cg}) \quad \text{…….(4)}$$

$$U_{ng} = \frac{1}{3}(U_{ag} + U_{bg} + U_{cg} - E_a - E_b - E_c) \quad \text{…..(5)}$$

In order to determine the ZCPs of the non-conducting phase back-EMF, the sensor less ZCP detection technique based on the virtual neutral point compares the terminal voltage with the virtual neutral point voltage. Taking the phase A as an example, when phase A is the non-conductive, the detected voltage difference in virtual neutral point based method can be obtained as(4.6).

$$U_{as} = U_{ag} - U_{sg} = \frac{1}{3}(2E_a - E_b - E_c) \quad \text{..(6)}$$

Similarly, phase B and C areas(7),respectively.

$$\begin{aligned} U_{bs} &= U_{bg} - U_{sg} = \tfrac{1}{3}(2E_b - E_c - E_a) \\ U_{cs} &= U_{cg} - U_{sg} = \tfrac{1}{3}(2E_c - E_a - E_b) \end{aligned} \quad \text{…..(7)}$$

By taking (2) into (6) and (7) and ignoring the third and above harmonic components that have less influence on the ZCPs detection, detailed actual detected voltage can be expressed as the equations at the bottom of the page. It is well known that odd harmonics are the main components in trapezoidal wave signals, while second or other even harmonics are very few. Therefore, when determining the impact of actual observed voltage on ZCP, only the fundamental and DC components remain after three or more harmonics are ignored. So, the real ZCPs that have been found can be acquired by setting them to zero. Furthermore, the junction of two neighboring back-EMFs, or the sites where Ea = Eb, Eb = Ec, and Ec = Ea, should theoretically be the optimal commutation point. The phase angle of the observed ZCPs that deviate from the ideal ZCPs, ϕz1−6, can be derived by comparing the phase connection between the discovered ZCPs and the ideal commutation points.

Comparison of different commutation points on instantaneous torque

The irregular current change rate brought on by the inductance during the commutation process can be disregarded due to the extremely low inductance value. As a result, only two phases are ever turned on during the square current driving mode.

Then, the instantaneous torque *Te* of the motor can be expressed as (8)

$$\begin{aligned} T_e &= \frac{E_x i_x + E_y i_y}{\omega_m} = p\frac{E_x i_x + E_y i_y}{\omega_e} \\ &= pk_e(e_x i_x + e_y i_y) = pk_e e_{xy}(\theta_e) i_m \end{aligned} \quad \text{……..(8)}$$

where, *ωm* is the mechanical speed, *p* is the pole pairs,

exy (*θe*) is the back-EMF difference shape function of phase*x* and *y*at position *θe*, and *im*is the DC-link current.

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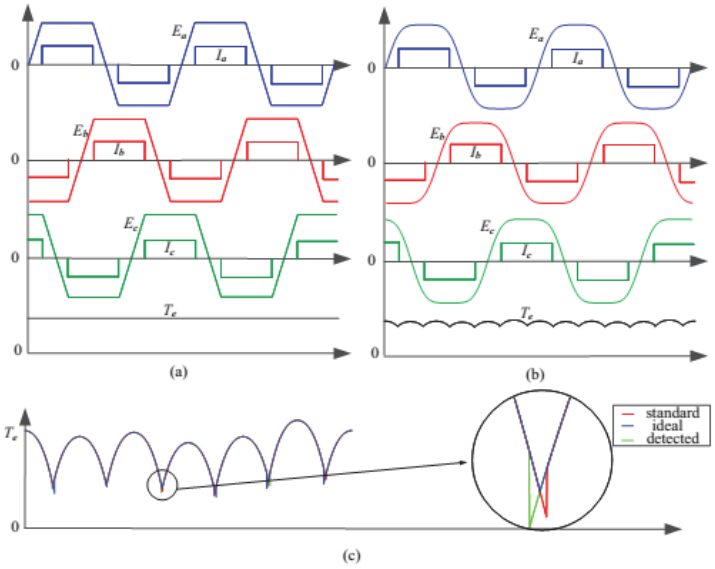

Fig 7 Currents and torque wave form of BLDCM driven by square wave current. (a) ideal back-EMF. (b) non-idealback-EMF.(c)torquewaveformscommutatedbydifferentcommutationpoints

Ignoring the commutation process, *AB* interval is defined as the phase *A* and *B* conduction interval, where current flowing from phase *A* to phase *B*. Similarly, each cycle can be divided into six intervals, namely *AB*, *AC*, *BC*, *BA*, *CA* and *CB*. The back-EMF difference shape function *exy* (θe) at different intervals are listed in Table4.1. For current closed-loop control, it can be seen that the back EMF models in each interval are different and nonlinear in Fig. 7, which makes it difficult to control the current wave form in the traditional square wave current drive mode. Fig.7(c) shows the instantaneous torque waveforms of the motor commutated according t commutation point by different methods. Because of the extremely low inductance value, the erratic current change rate caused by the inductance during the commutation process may be ignored. Consequently, in the square current driving mode, only two phases are ever activated.

C. Optimal commutation control

The motor that commutated in accordance with the optimal commutation point had the lowest torque fluctuation as well as the highest average torque and efficiency among the three commutation points, according to the data shown above. Furthermore, the primary cause of commutation deviation in various signal processing circuits is the phase delay produced by LPF, in addition to the influence of non-ideal back EMF on the phase deviation of ZCP detection method. LPF cut-off frequency used to eliminate noise interference to avoid false detection is very low, so a large phase delay is introduced. Based on the analysis of commutation deviation, this paper presents a new optimal commutation method. An enhanced commutation compensation approach that takes non-ideal back-EMF factors and low-pass filter delay into account is the optimal commutation method.

The proposed optimal commutation method consistsofthefollowingsteps:1)Estimate LPF delay phase: The LPF is generally approximated to a first-order inertia unit as $LPF(s) = s+ \omega\omega\ c\ c$, $\omega c$is the cutoff frequency speed, then LPF delay phase $\phi\ LP\ F$ can be estimated according to the phase characteristics $\phi\ LPF$=−arctan($\omega e/\omega c$).2) Calculatedeviationphaseϕz1−6:firstly,obtaintheactualback-EMFwaveformsbyoffline measurement at constant speed and normalize back-EMF wave form function.

Then, a 1-2-9-1 structure, 4 layers feed-forward backpropagation neural network is used for fitting the accurate back-EMF waveform function. By applying Fourier decomposition to the fitted back EMF function, the back-EMF harmonic coefficients can be derived.

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4. SIMULINKMODEL

Figure8 show the resonant based high gain converter with half bridge rectifier in the front end followed by high frequency transformer with the resonant cell and voltage doublers circuit at the end

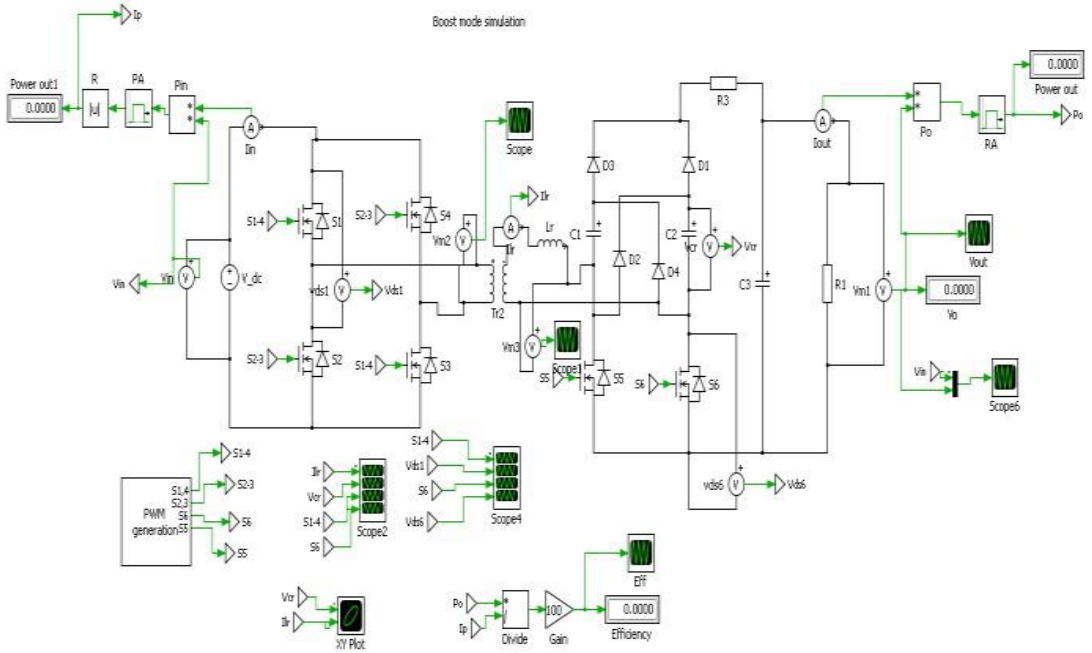

Figure 8 illustrates the Simulink model of the Resonance-based High-Gain Converter.

The PWM signal, as well as the input and output voltages of the switches in the front full bridge rectifier and the back-end voltage multiplier circuit, are displayed in Figure 8. The resonant inductor, resonant capacitor, and driving voltages of S1 and S6 in the boost mode steady-state waveforms are also depicted. It is noted that dφP<1, and the converter operating in boost mode is indicated by the driving signal of S1, vGS1, observed to lag behind the driving signal of S6, vGS6.

The primary side switches S1 & S4 operate with a duty cycle of 50%, whereas S2 & S3 operate with a phase shift control of 1μs with 30% duty. The secondary side switches operate with a 45% duty cycle. The primary conversion becomes more efficient once the secondary becomes zero due to the soft switching patterns for the primary side switch S1 and the secondary side switch S6, which work with static zero voltage switching patterns.

Simulation Result

In comparison to a typical Boost converter with an equivalent gain, this research offers a high step-up topology featuring minimal switch voltage stress and lower magnetic energy. The conversion process explores both magnetic coupling and a charge pump mechanism to efficiently transfer power.

The conversion efficiency (power stage only) was calculated by measuring input and output powers using digital millimeters (Keysight 34461A) for input/output voltages and output current, while the input current was directly read on the DC power supply Chroma 62050P-100-100. The overall relative error on the efficiency calculation is lower than 0.5%, with the main contribution coming from the input current measurement (0.1% of reading plus 0.1% of range).

Measured efficiencies above 95% are achieved at nominal power except at the lower part of the input voltage range (Vg=42V). Here, the slight efficiency reduction is caused by the different operating conditions mentioned above, according to which Tr1/2 > (1−Dmax)Ts, causing an increase of S1 turn-on losses, as revealed by the vDS2(t) waveform in Fig. 7a. At lower output current values, the efficiency remains above 90% down to approximately one-tenth of the nominal power, as revealed by the measurement reported in Fig. 13 for two different input voltage values (Vg = 44V and Vg =48V).

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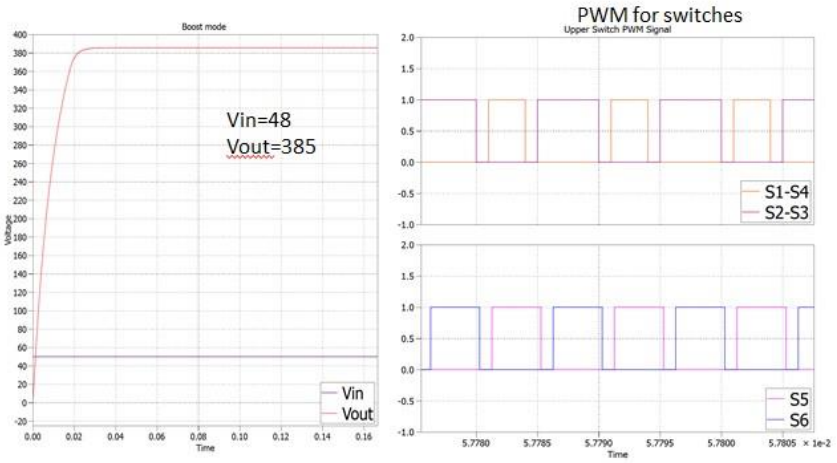

Fig 9: Boost Mode Output

The relative losses distribution between the different components was calculated based on the stress analysis reported in Section IV at the nominal operating point, and the result is shown in Fig. 14. The total power loss was estimated as P Estimated Loss = 10W, lower than the measured one P Measured Loss = 15.8W. Turn-off switching losses have been considered as well, even though the commutation time intervals are very difficult to predict.

This is because the switching node transition is affected by the huge MOSFET's output capacitance (roughly 3.4nF each), which acts as a lossless snubber, especially at the S2 turn off, where the switched current is quite low (≈−2.5A from Fig. 8). However, the forecasted total S1 losses of 1.37W are not unrealistic since the temperature measured on the device package in the same operating point was 83°C without forced air circulation (ambient temperature TA ≈ 20°C). With a thermal resistance from junction to ambient of the TO263-7 package ranging between 40K/W with 6cm^2 of cooling area and 62K/W with minimal footprint, it means a dissipated power in the range 1 to 1.6W. Turn-on switching losses have been neglected for both switches, thanks to the quasi-square-wave operation imposed by a proper selection of the magnetizing inductance Lb, even if this condition is not completely met for S1, as can be inferred from the rising edge of voltage vDS2(t) in Fig. 7b. However, the small switched current and residual voltage (≈ 10V) give a negligible contribution to the overall losses. The core loss was estimated based on the manufactured at a of the used N87 ferrite material.

Conclusion

The devices' high RMS current value following—a necessary trade-off for having the lowest possible switch voltage stress—makes controlling any parasitic resistance in the current channel essential to preventing conduction losses. Because of this, additional lower value capacitors were connected in parallel to implement the input and buck stage capacitances, as table II reveals. Due to the fact that the resonant current id automatically turns off the SiC diodes in the experimental prototype, they are not the ideal option for this circuit. Si devices with lower voltage ratings and, hence, lower voltage loss could be employed for improved overall efficiency, given their voltage stress (see table III).

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