International Research Journal in Global Engineering and Sciences. (IRJGES)
ISSN : 2456-172X | Vol. 5, No. 4, December - February, 2021
Pages 25-32 | Cosmos Impact Factor (Germany): 5.195
Received: 02.12.2020 Published: 28.02.2021

IMPLEMENTATION OF LOW POWER 17-TRANSIST OR TRUE SINGLE-PHASE CLOCKING FLIP –FLOP DESIGNS WITH 45 NM CMOS TECHNOLOGY

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Abstract:
Flip-Flops (FFs) serve as fundamental storage components extensively employed in digital system designs, particularly in structures involving pipelining and modules constructed by FFs. However, FFs contribute significantly to both the power consumption and chip area of digital systems. Consequently, there arises a demand for FF designs that prioritize low power consumption and reduced area. In this paper, a low-power 17-True Single-Phase Clock (TSPC) flip-flop method is proposed, which has gained widespread usage in advanced design.
The proposed flip-flop operates in 45 nm CMOS and features a logic structure of the TSPCFF of master-slave type. The master stage comprises static CMOS logic, while the slave stage utilizes a mixed combination of static CMOS logic and complementary pass transistor logic. This design ensures that the TSPC FF circuit remains fully static during operation, thus preventing leakage power dissipation.
The proposed TSPC FF design optimizes a 17-transistor logic structure reduction flip-flop (LRFF) concerning area and power consumption without compromising functionality. To validate the design, three FFs—Transmission Gate based Flip-Flop (TGFF), LRFF, and the proposed TSPC FF—are implemented and simulated using gpdk 45 nm technology library with a supply voltage (Vdd) of 1V and clock frequency of 500MHz in DSCH and MICROWIND tool.
Keywords: TSPC, VLSI, Flip-Flop, RAM, ROM, SRAM.

I. Introduction:

Two essential characteristics of CMOS devices are high noise immunity and low static power consumption. The CMOS arrangement draws significant power only momentarily during transitions between on and off states due to one transistor of the pair always being off. Consequently, CMOS devices generate less waste heat compared to other logic types, such as transistor-transistor logic (TTL) or N-type metal-oxide-semiconductor logic (NMOS). CMOS also enables high logic density on a chip, making it the most widely used technology in very-large-scale integration (VLSI) chips.
The term "CMOS" refers to both a specific style of digital design and the array of techniques used to implement that electronics on integrated circuits (chips). CMOS circuits dissipate less power than logic families with resistive load. As this advantage has become increasingly important, CMOS processes and variations have come to dominate, with the majority of modern integrated circuit manufacturing utilizing CMOS processes. CMOS circuits employ a combination of p-type and n-type metal-oxide-semiconductor field-effect transistors (MOSFETs) to implement logic gates and other digital circuits. While CMOS logic can be demonstrated with discrete devices, commercial CMOS products are integrated circuits composed of billions of transistors of both types on a rectangular silicon chip ranging from 10 to 400 mm2. CMOS always uses enhancement mode MOSFETs.

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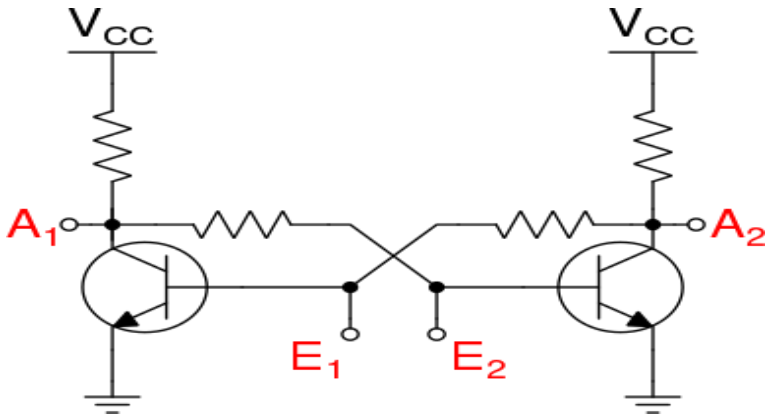

Figure 1: Traditional Flip-Flop Circuit

Flip-flops are essential storage elements in digital system design, commonly used to implement pipelining structures. However, more than 50% of the random logic power in a System-on-Chip (SoC) chip is consumed by their unnecessary transitions of internal nodes when the output and input are in the same state. Various low-power techniques have been discussed, but many of them involve increasing transistor count, leading to size increase which is cost-prohibitive.

The conventional Transmission Gate Flip-Flop (TGFF) typically consists of two clock buffers and inverters, consuming power in every clock cycle. To address this, a topology of differential master-slave flip-flops has been recognized, aimed at reducing clock buffer activity and data activity.

With the rise of the Internet of Things (IoT) and wearable devices, the demand for ultra-low power SoC chips is increasing. One effective method to reduce power consumption is to decrease voltage, leading to the examination of circuit operation at near-threshold and sub-threshold voltages. Digital circuit designs often utilize extensive flip-flops for data buffering and pipelining, and the capacity of flip-flop design significantly impacts overall power consumption and chip area.

The proposed design optimizes a 17-transistor True Single-Phase Clock (TSPC) Flip-Flop, derived from an 18-transistor TSPC FF. This new flip-flop, referred to as True Single-Phase Clocking Flip-Flop (TSPCFF), is fully static, contention-free, and operates on single-phase clocking. The device count is almost the same as a TGFF, with a layout size increase equivalent to a single poly-pitch increase in 45nm technology. An additional advantage of the TSPC topology is its clarification of the "hold-time path" compared to a regular TGFF.

True Single Phase Clock (TSPC) Flip-Flops are unique in their ability to operate quickly and consume low power. The purpose of a clocked storage component is to capture data at a specific moment in time and retain it as long as necessary for the advanced framework. Near-threshold computing has brought about significant improvements in every aspect. For many CMOS designs, energy consumption reaches a minimum in the Near Threshold Voltage (NTV) regime, which is orders of magnitude lower than super-threshold operation.

However, voltage scaling may lead to degradation of frequency across all performance-constrained or single-threshold applications. Enabling digital design to operate over a large voltage range is crucial for achieving optimal energy efficiency, while effectively managing application execution demands exploiting the full potential of NTC. Multilayered co-optimization strategies that cut across devices, architecture, design, circuit methodology, and tool flows, along with techniques of fine-grain power management, are necessary to realize NTC circuits in scaled CMOS process nodes.

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True Single Phase Clock Architecture

Most integrated circuits (ICs) typically utilize a clock signal to synchronize various components of the circuit operating at a rate slower than the worst-case internal delays. In some cases, more than one clock cycle is required to complete an intended operation. As ICs become more complex and powerful, the challenge of providing precise and synchronized clocks to all circuits becomes increasingly difficult.

A prime example of such complex chips is the microprocessor, the central component of modern computers, which relies on a clock generated from a crystal oscillator. The main exceptions to this synchronous clocking are asynchronous circuits, such as asynchronous CPUs.

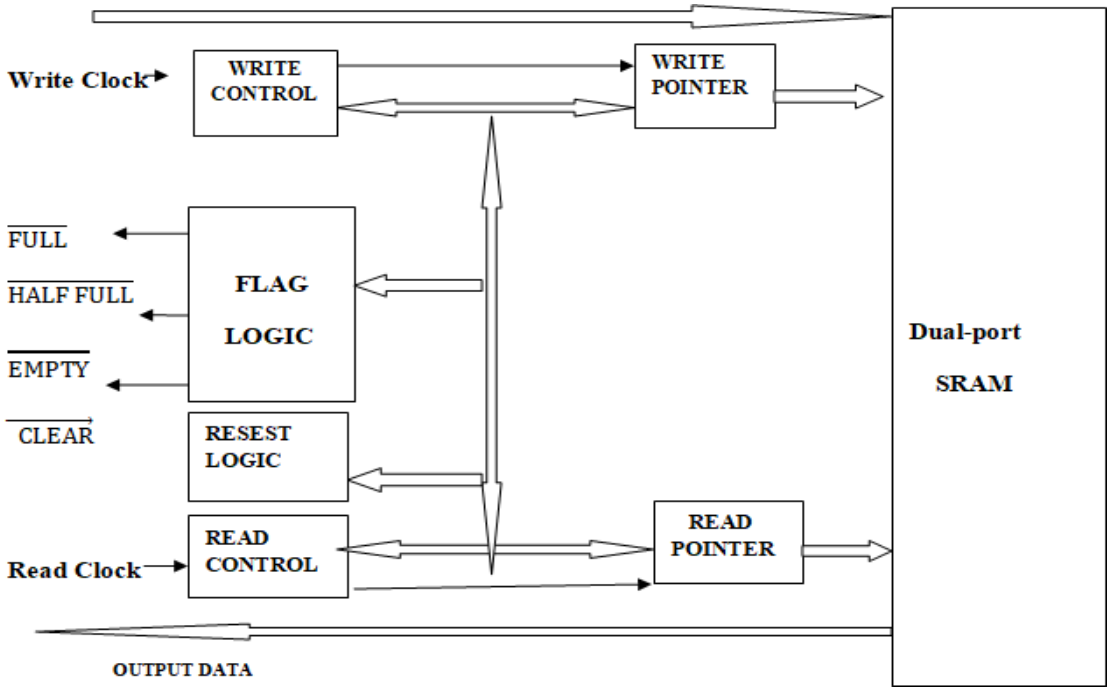

Figure 2: Block Diagram of FIFO with Storage

In Figure 2, addressing the issue of long fall-through time in large FIFOs involves avoiding the movement of data words through all memory regions. This problem is resolved by an indirect FIFO concept, where the memory address of the incoming data is stored in the write pointer. The location of the first data word in the FIFO to be read out is stored in the read pointer. Initially, after reset, both pointers indicate the same memory region. After each write operation, the write pointer is set to the next memory region.

The design process involves the following steps:

1. **Design in DSCH Software**: Firstly, design the circuit using available components in the DSCH software and establish connections between them as per requirements.
2. **Simulation**: Run simulation to observe the output, typically in terms of LED glow or other indicators. If the input and clock signals are active and the LED glows as expected, the designed circuit provides the correct output. Otherwise, errors in the circuit design need to be addressed.
3. **Save Design and Generate Verilog File**: Save the design and generate a Verilog file. This Verilog file is automatically generated and will be used in the subsequent steps.
4. **Compile and Layout Generation**: Open Micro wind software, compile the Verilog file, and

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generate the CMOS layout. Calculate parameters and compare results.

This design proposes a 17-transistor SPC (17TSPC), which is an SPC Flip-Flop with only 17 transistors (the lowest reported for a fully static, contention-free SPCFF) with a novel master-slave configuration (refer to Figure 3). Simulation results depict the TCFF internal node voltage at (a) VDD=1.2V and (b) VDD=0.6V when D is rising at CK=0. This topology, with a simplified structure, delivers a 20% reduction in cell area compared to a TGFF in 45-nm CMOS.

The design demonstrates EDA compatibility and exhibits benefits at both circuit and system levels. Initially simulated, it was then experimentally validated at 0.7V and 25°C, with various data activity rates (a), showing that the proposed 17TSPC achieves reductions of 68% and 73% in overall (Pa=10%) and clock dynamic power (Pa=10%), respectively, and 27% lower leakage compared to TGFF. Furthermore, unlike TCFF, measurements indicate superior performance with 17TSPC.

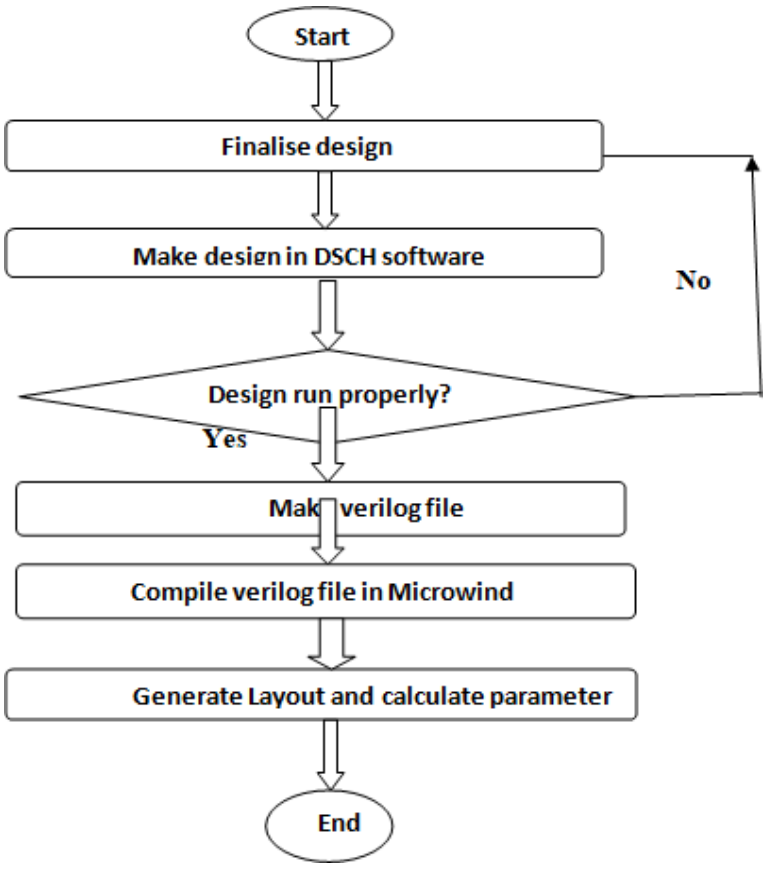

Figure 3: Flow Chart

The proposed design is compared with two other static FF designs: the TGFF and the S2CFF. It's important to note that a True Single Phase Clock (TSPC) based FF design using 17 transistors is proposed.

Simulation and Result

The simulation studies involve the deterministic TSPC circuit, as shown in Figure 4. The proposed TSPC circuit is implemented using DSCH-Microwind software.

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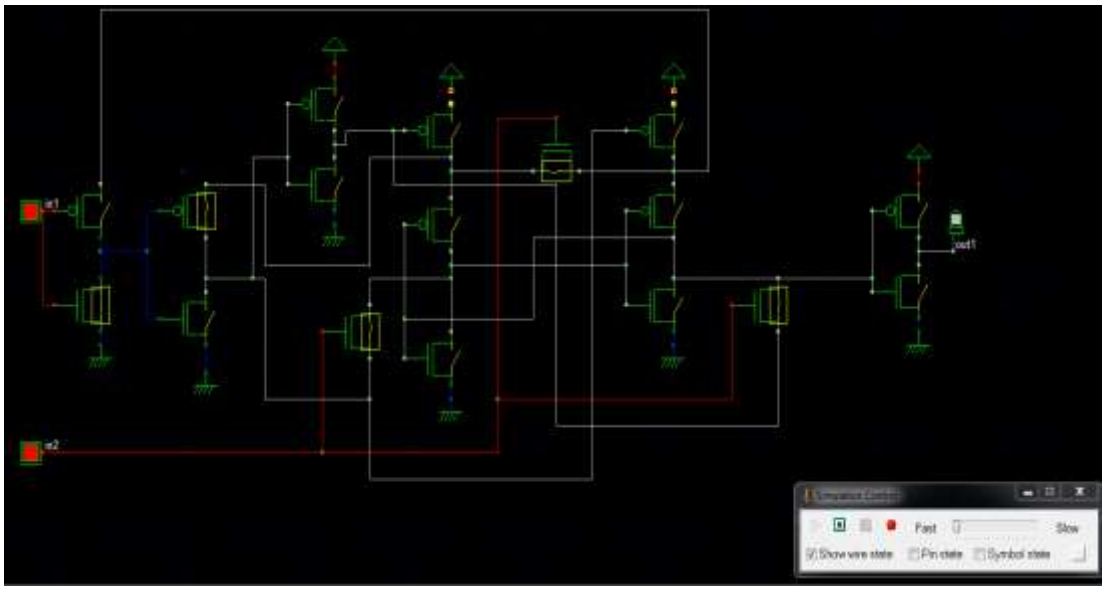

Figure 4: Working of True Single-Phase Clock Flip-Flop

Figure 4 illustrates the design of the True Single-Phase Clock Flip-Flop (TSPCFF). It shows the transistor-level single-phase clocked AND gate, with PMOS and NMOS components used in the circuit. When the clock (clk) signal is 1 and the data (D) input is also 1, the output (Q) is 1.

Table 1: Truth Table of TSPCFF

Clk	D	Q
0	0	Q
0	1	Q
1	0	0
1	1	1

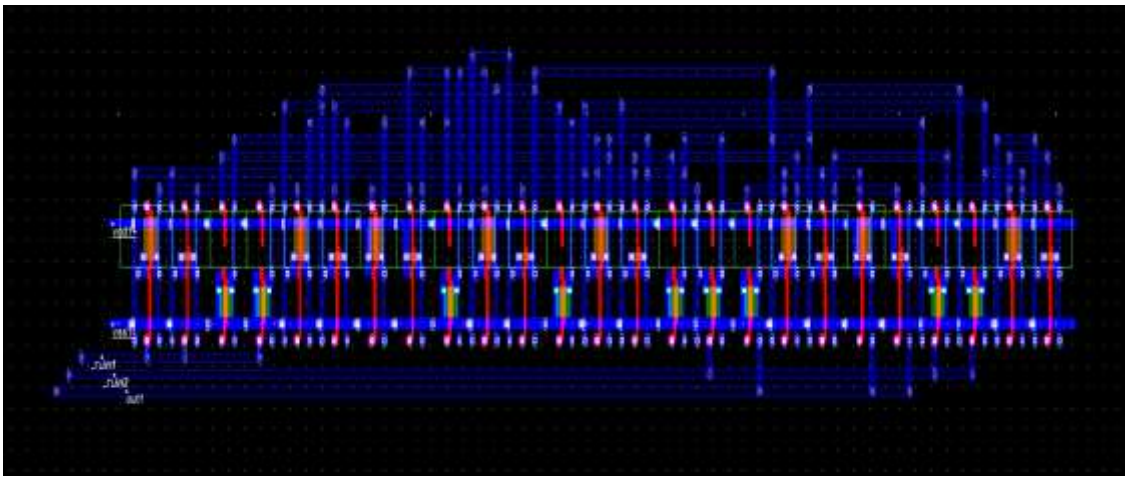

Figure 5: Proposed TSPC Design Circuit Layout

Figure 5 presents the CMOS layout design of the True Single-Phase Clock Flip-Flop (TSPCFF). It

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includes various metal layers, PMOS, NMOS, and contact points.

Table 2: Simulation Parameters of Proposed TSPC

Sr. No	Parameters	Value
1	Area	374.0µm2
2	Power	3.38µw
3	Delay	5ns
4	Power Delay Product (PDP)	625.28
5	Rise Time	0.025ns
6	Fall Time	0.025ns

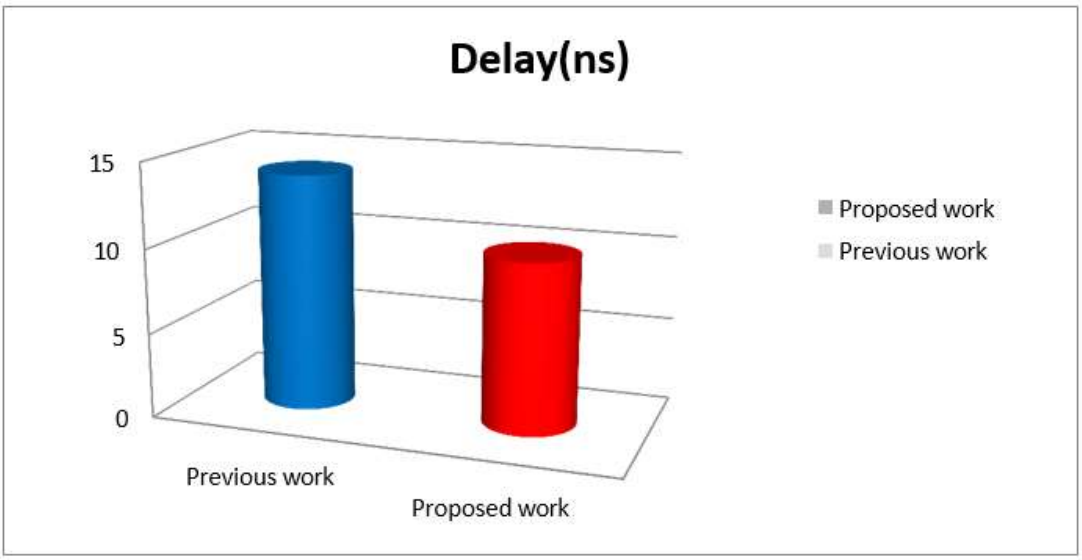

Figure6: Delay plot of previous vs proposed design

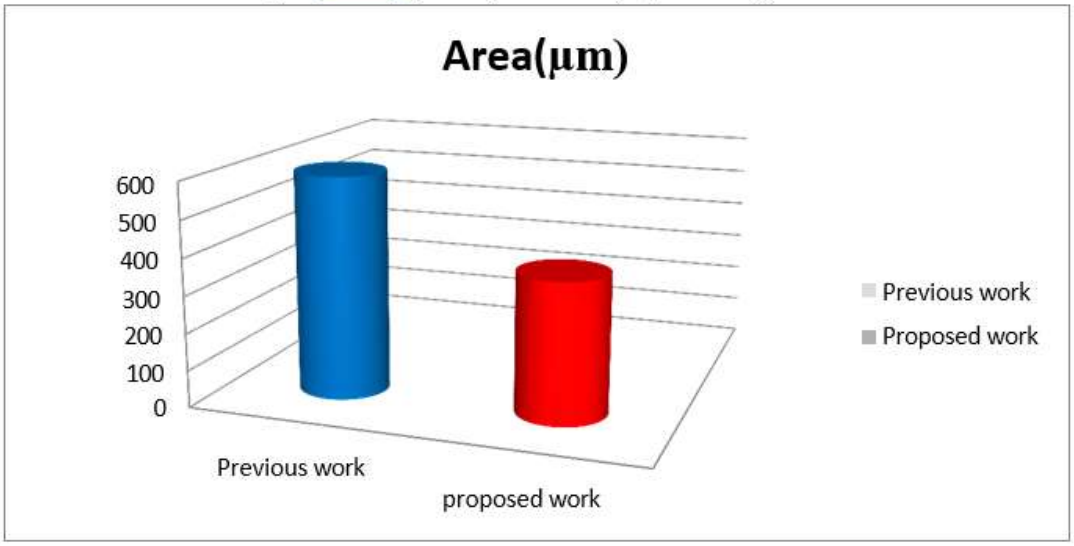

Figure7: Area plot of previous vs proposed design

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Therefore, after observing all simulated results and parameter values, it is evident that the proposed design outperforms the previous design. Improvements in parameters such as reduced transmission time and latency are noted.

The implementation and simulation of the proposed design were carried out using DSCH-MICROWIND software. DSCH software offers various menus and help bars where different gates, power supplies, grounds, etc., are available. Microwind software also provides functionality to convert DSCH designs into Verilog files and layout diagrams.

Conclusion

This paper presents a new flip-flop, referred to as the Static Single-Phase Contention-Free Flip-Flop (SPCFF), with the lowest reported number of transistors (17). It demonstrates a reduction in cell area compared to the conventional TGFF. While some penalty is observed, the low-power usage and utilization of single-phase clocking in the TGFF contribute to layout size increases corresponding to a single poly-pitch increase in 45nm technology.

To achieve reliable, energy-efficient operation across a wide operating voltage range, single-phase clocking is utilized, avoiding toggling of internal clock inverters and the associated power penalty. A brief summary of the proposed 17TSPC and a comparison with prior works are presented. Therefore, the proposed 17TSPC exhibits better power characteristics than previous designs.

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