International Research Journal in Global Engineering and Sciences. (IRJGES)
ISSN : 2456-172X | Vol. 7, No. 2, June 2021 – August 2021 | Pages 1-10

Power Flow of MTDC Using Droop Control & Impact of DC Voltage Drops

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Abstract—This paper investigates the ramifications of DC transmission voltage drops on the distribution of DC grid balancing power under the application of DC voltage droop control. In a multiterminal VSC-HVDC (MTDC) system, variations in DC line voltage due to drops lead to nonuniform adjustments in DC bus voltages, thereby impacting the allocation of instantaneous balancing power. The influence of DC voltage droop constants determines the extent to which these voltage drops affect the sharing of balancing power across the DC grid. An analytical expression is formulated to estimate the distribution of balancing power, accounting for DC line voltage drops. A five-terminal MTDC system is simulated using PSCAD to demonstrate the effects of DC line voltage drops and validate the proposed analytical expression.
Index Terms: DC grid, droop control, multiterminal VSC-HVDC (MTDC), voltage source converter high-voltage DC transmission (VSC-HVDC).

NOMENCLATURE

- VSC: Voltage source converter
- HVDC: High-voltage DC transmission
- MTDC: Multiterminal VSC-HVDC

INTRODUCTION

In recent years, significant research efforts have been directed towards the development of VSC-based multiterminal HVDC systems, particularly driven by the expansion of offshore wind farms, such as those in the North Sea region. Multiterminal VSC-HVDC (MTDC) systems, also referred to as DC grids, offer advantages including reduced transmission losses, enhanced control flexibility, synchronization of asynchronous grids, and ease of integrating new VSC-HVDC terminals into existing MTDC setups.

Control strategies proposed in the literature for MTDC systems can be broadly classified into two groups: constant DC voltage control schemes (often termed master-slave control schemes) and DC voltage droop control schemes. The operational principle of constant DC voltage control, also known as the master-slave scheme, has been extensively discussed in prior works. However, one drawback of this approach is its dependency on the normal operation of the DC voltage regulating terminal (i.e., the master terminal). In contrast, DC voltage droop control involves two or more terminals participating in DC voltage regulation, thereby sharing the responsibility of instantaneous power balancing among them. This approach is considered more reliable as it ensures continued operation of the MTDC system even if one terminal is disconnected.

While the basic working principle of DC voltage droop control in MTDC systems has been explored, the impact of DC line voltage drops on primary DC grid power balancing has not been thoroughly analyzed. This paper aims to address this gap by investigating how DC line voltage drops influence the distribution of balancing power in droop-controlled MTDC systems. The paper also sheds light on the subtle yet

significant influence of DC line voltage drops on balancing power distribution, which is crucial for optimizing the operation of MTDC systems.

DC bus voltage variations are dependent on the topology and line conductances of the DC grid, resulting in different responses from converter terminals to changes in power flow across various locations of the grid. Additionally, the chosen DC voltage droop constants also influence the severity of the impact of DC bus voltage variations on the distribution of balancing power.

This paper compares two mathematical models for DC grid power balancing to understand the influence of DC line voltage drops on power flow. The first approach neglects DC line voltage drops, while the second one, which is the main contribution of this paper, considers these drops to describe the system interaction more accurately. A five-terminal VSC-HVDC system is simulated in PSCAD, and the results are compared with the estimations from the two mathematical models. It is demonstrated that the proposed model (the second approach) accurately describes the droop interactions in the DC grid and serves as a useful tool to understand the influence of DC line voltage drops on the power flow of DC grids.

This paper is outlined as follows:

- In Section II, the different types of VSC-HVDC control are discussed.
- Section III discusses the distribution of DC grid balancing power in an ideal lossless DC grid in the presence of DC voltage droop control.
- In Section IV, the impact of DC line voltage drops is discussed.
- Section V discusses the proposed analytical expression for estimating the distribution of balancing power in DC voltage droop controlled DC grid systems.
- Section VI presents simulation studies to demonstrate the impacts of DC voltage line drops and to validate the proposed analytical estimation method.
- Conclusions are drawn in Section VII.

II. VSC-HVDC TERMINAL CONTROL ![

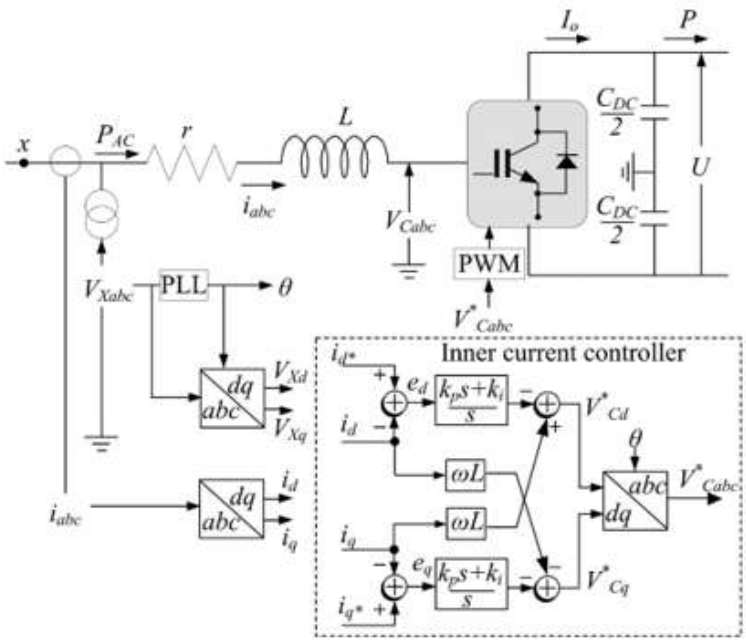


Fig.1.SchematicdiagramoftheVSCcontroller.

TABLEI
LISTOFSYMBOLSINFIG.1

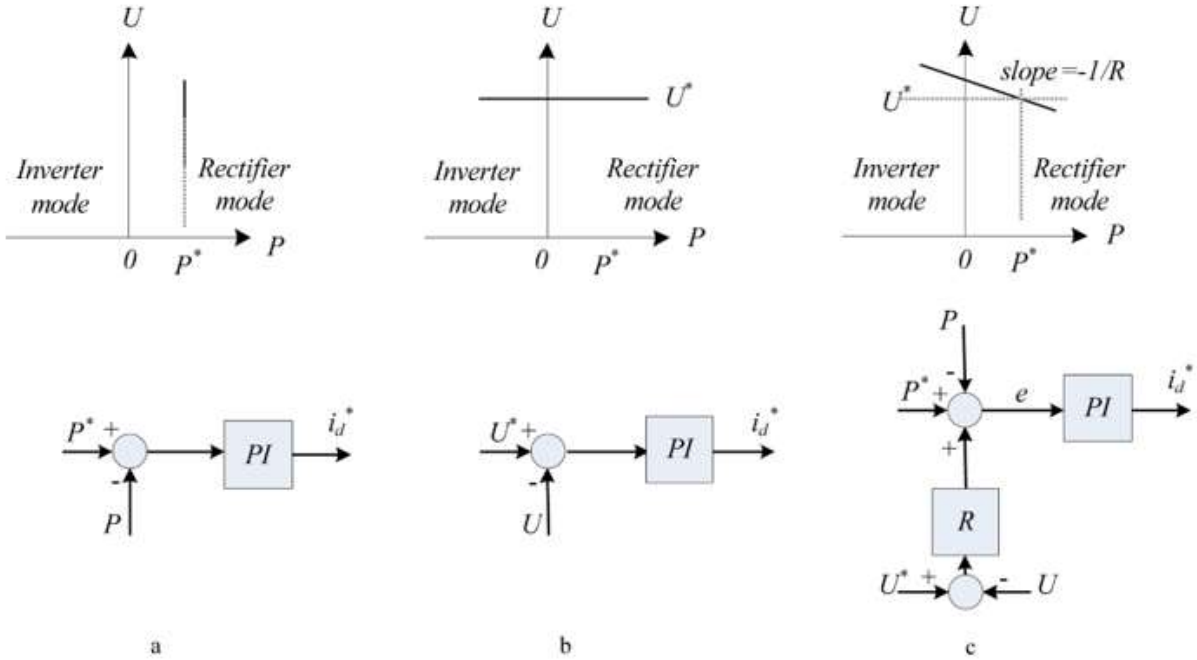
P	DC bus power measurement of the converter;
P_{AC}	AC side converter power measured at PCC;
PLL	Phase locked loop;
PWM	Pulse width modulator;
i_{abc}	3-phase AC current measured at PCC;
V_{Xabc}	3-phase AC voltage measured at PCC;
V_{Cabc}	3-phase AC voltage output of VSC;
V^*_{Cabc}	3-phase AC voltage reference for VSC;
V_{Xd}, V_{Xq}	AC voltage at PCC in dq reference frame
V_{Cd}, V_{Cq}	AC voltage of VSC in dq reference frame
V^*_{Cd}, V^*_{Cq}	AC voltage reference for VSC in dq reference frame
I_o	DC current of VSC behind DC capacitor;
U	DC voltage measurement (pole to pole);
ω	Synchronous frequency in rad/s;
L, r	Series filter inductance and resistance;
C_{DC}	DC bus capacitance;
k_p, k_i	Proportional and integral gains of inner controller
abc/dq	abc to dq transformation
dq/abc	dq to abc transformation
e_d, e_q	Error signals of PI controllers of the inner current loop

TABLE I LIST OF SYMBOLS IN FIG. 1

A. Basic VSC Controller The most commonly used control approach for VSC is the decoupled-axes (d-q axes) oriented control, where the d-axis of the synchronously rotating reference frame is aligned to the voltage phasor of phase-A measured at the point of common coupling (PCC) (point in Fig. 1). This

alignment also implies that the quadrature axis (q-axis) component of the voltage measurement becomes zero. The sign convention used here for the power and current measurements of the converter ensures that power/current measured at a converter terminal is positive if it flows from the AC grid to the DC grid via the converter station, with positive corresponding to rectifier mode of operation and negative corresponding to inverter mode of operation.

The voltage–current relation in Fig. 1 is given by:
$Aftertheabc/dqtransformations$,(1)$takestheformof$(2)*Aftertheabc/dqtransformations*,(1)*takesthef ormof*(2)



![Fig. 2 DC terminal control configurations and the corresponding DC voltage versus power characteristics. (a) DC bus power controller (b) DC voltage regulator (c) DC voltage droop controller](Insert URL of Fig. 2)

The apparent power and real power measured at PCC are expressed as:
*S*PCC=*P*PCC+*jQ*PCCSPCC=*P*PCC+*jQ*PCC
where *P*PCC and *Q*PCC refer to apparent power and real power of the converter. *V*d and *I*d refer to direc t-axis (d-axis) voltage and direct-axis current of the converter measured at PCC.where *P*PCC and *Q*PCC refer to apparent power and real power of the converter. *V*d and *I*d refer to direct-axis (d-axis) voltage and direct-axis current of the converter measured at PCC.
Reactive power/AC voltage control is not the focus of this paper and will not be discussed here. Depending on the mode of operation, the active current reference *I*ref*I*ref is used to control active power or DC bus voltage of the VSC.

B. DC Voltage and Power Control Modes
A VSC-HVDC terminal, hereafter simply referred to as a DC terminal, may have one of three control modes: constant power mode, constant voltage mode, or droop mode of control. The DC voltage versus power characteristic curve of the constant power mode DC terminal is shown in the top of Fig. 2(a), where *P*d*P*d is the power axis and *V*d*V*d is the DC bus voltage.

Constant DC voltage control is represented by Fig. 2(b) (bottom), where VrefV ref and VdVd refer to DC voltage reference and actual DC bus voltage, respectively. A DC terminal which regulates DC voltage will have a DC voltage versus power characteristic curve shown in Fig. 2(b) (top).
DC voltage droop control can be seen as a combination of the first two types of VSC-HVDC control. It tries to control power to its reference level while at the same time contributing some balancing power. Since these two actions are somewhat contradicting (i.e., power control and DC voltage control), one action happens at the cost of steady-state deviations for the other. DC voltage droop control is shown in Fig. 2(c) (bottom), and the corresponding PdPd versus VdVd characteristic is shown in Fig. 2(c) (top).
In Fig. 2(c) (bottom), the symbol kPkP refers to the DC voltage response (analogous to the frequency response of synchronous generators in AC grids) and has the unit of MW/kV. The slope is often given in terms of the DC droop constant kdkd, which is the ratio of change in DC bus voltage to the corresponding change in converter power both in per-units. It could also be defined as the change in DC voltage in per-unit that results in a 100% change in converter power flow. The DC voltage droop constant kdkd and the DC voltage response kPkP are related to each other by:

kP=kd×Prated$V$rated$k$P=kd×Vrated$P$rated
Where Prated$P$rated and Vrated$V$rated refer to rated power and rated DC voltage of the DC terminal, respectively.

From the DC voltage droop controller in Fig. 2(c) (bottom), the error signal ΔVdΔVd is given by:
ΔVd=Vref−VdΔVd=Vref−Vd
At steady state, the relation between DC voltage and converter power then becomes:
ΔPd=kd×ΔVdΔPd=kd×ΔVd

It could be noted that the steady-state characteristics in constant power control mode and constant DC voltage control mode could be represented by DC voltage droop controllers with kd=0kd=0 (i.e., kPkP) and kd=∞kd=∞ (i.e., kP=0kP=0), respectively. For analytical purposes, a large (but finite) value of kdkd could sufficiently represent steady-state behavior in constant DC voltage control mode.
In the absence of DC voltage error signal, the converter power will be the same as the power reference without any steady-state deviations. Hence, for precise control of power, the DC voltage reference in Fig. 2(c) (bottom) should be assigned according to results from load flow analysis conducted for the entire DC grid. For further details about DC grid load flow analysis, the reader is referred to [9].
Now let us consider an initial steady-state operating point of the controller in Fig. 2(c) (bottom) with input and output variables represented by the superscript "1," i.e., Pd1Pd1, Vref1Vref1, Vd1Vd1, and PPCC1PPCC1. The input/output variables at another steady-state point could be expressed in terms of the initial steady-state conditions expressed by ΔPdΔPd, ΔVrefΔVref, ΔVdΔVd, and ΔPPCCΔPPCC. Substituting ΔVd1ΔVd1 into ΔPd1ΔPd1 yields the relation:
ΔPd1=kd×ΔVd1ΔPd1=kd×ΔVd1
Furthermore, we assume that during initial steady-state conditions, all error signals are zero, as in ΔVref1=ΔPPCC1=0ΔVref1=ΔPPCC1=0. Substituting ΔVd1ΔVd1 into ΔPd1ΔPd1, we obtain:
ΔPd1=kd×ΔVd1ΔPd1=kd×ΔVd1
From this, the change in output of the droop controller due to changes in inputs becomes:
ΔPd1=kd×ΔVd1ΔPd1=kd×ΔVd1
In matrix form, this could be rewritten as:
ΔPd=kd×ΔVdΔ**Pd**=kd×Δ**Vd**
Other vectors such as Pin**Pin**, $Pout$**Pout**, and Vd**Vd** are also defined in a similar manner. The vector, which refers to power flow into the DC grid via the DC terminals, is given by:
Pin=Y∘Vd**Pin**=**Y**∘**Vd**
where Y**Y** refers to the admittance matrix of the HVDC grid, and the symbol ∘∘ is the entry-wise (point-to-point) matrix multiplication operator, also called Hadamard product operator. Differentiation of the

power flow equations of individual terminals with respect to the nodal voltage vector results in the Jacobian matrix J**J** of the DC grid. This is mathematically given by:

$J=\partial Pin\partial Vd$**J**$=\partial$**Vd**$\partial$**Pin**

If the HVDC grid has an initial state given by $Vd1$**Vd1**, the linearization of power flow equation around the initial steady-state point is given by:

$\Delta Pin=J\times\Delta Vd\Delta$**Pin**=**J**$\times\Delta$**Vd**

Hence, the relationship between the vectors representing small DC voltage variations $\Delta Vd\Delta$**Vd** and small nodal power variations $\Delta Pin\Delta$**Pin** is given by:

$\Delta Pin=J\times\Delta Vd\Delta$**Pin**=**J**$\times\Delta$**Vd**

If the vector $\Delta Pin\Delta$**Pin** is known, the voltage vector $\Delta Vd\Delta$**Vd** could be found by:

$\Delta Vd=J-1\times\Delta Pin\Delta$**Vd**=**J**$-$**1**$\times\Delta$**Pin**

Care should be taken while computing $J-1$**J**$-$**1** to avoid the singularity condition during the inverse matrix calculation. The inverse matrix gets closer to singularity if computed close to a flat DC voltage profile (i.e., when all DC bus voltages are very close to each other and DC grid power flow approaches zero). Once computed at a suitable operating point, the Jacobian matrix could be applied for a wider range of operations with negligible errors.

Equation (11) is rewritten in vector form as:

$\Delta Pd=k$d$\times\Delta Vd\Delta$**Pd**$=k$d$\times\Delta$**Vd**

indicating the relationship between changes in power references of the DC terminals with the resulting steady-state changes in injected powers at each of the terminals. From (24) and (27), the DC voltage change becomes as:

$\Delta Vd=\Delta Vd1+\Delta Vd2\Delta Vd=\Delta Vd1+\Delta Vd2$

Comparing (18) and (27), the differences in the two equations result from the differences between the constant matrices J**J** and $J-1$**J**-1. As discussed in Section III, the matrix J**J** is independent of DC grid topology since a lossless grid was assumed to establish the mathematical relation. In contrast, in the proposed analytical method, the constant matrix $J-1$**J**-1 is dependent upon DC line resistances and hence upon DC grid topology. This is reflected by the presence of the DC Jacobian matrix J**J** in (27). Due to the line voltage drop considerations, the proposed method gives an accurate mathematical model of the interaction between power control reference changes and the resulting observed power flow pattern in the DC grid.

V. EFFECT OF INCREASING/DECREASING DC VOLTAGE DROOP CONSTANT

From (5), it could be seen that the DC droop constant in physical units (i.e., kdkd, the DC voltage response in MW/kV of a single terminal) could be changed by changing either the rated power Prated$P$rated, rated DC voltage Vrated$V$rated, or the DC droop constant (i.e., kdkd). Since Prated$P$rated and Vrated$V$rated are fixed parameters for an already existing DC grid, kdkd is the only means for changing the value of kdkd. By following the same practice as in frequency droop control of synchronous generators, it may be reasonable to assign all DC terminals participating in DC voltage control the same value of kdid.

Now, consider an initial value of the DC voltage response vector $kP1$**kP1**, such that a new DC voltage response vector kP**kP** is given by:

$kP=\alpha\cdot kP1$**kP**$=\alpha\cdot$**kP1**

where $\alpha\alpha$ refers to a scaling factor by which we want to vary the droop constants of the entire DC grid. Then the initial total DC voltage response will be given by $\sum kP1\sum$**kP1**. Substituting kP**kP** into the definition of KP**KP** in (15), we obtain:

$KP=$diag(kP)**KP**=diag(**kP**)

where diagdiag refers to a mathematical operator which transforms a vector into a diagonal matrix. Substituting (30) into the definition of Y**Y**, we obtain:

$Y=G\times$diag$(kP)\times GT$**Y**=**G**$\times$diag(**kP**)$\times$**G**T

Equation (26) could further be simplified as:
$Pin=Y\circ Vd$**Pin**=**Y**$\circ$**Vd**
$Pin=(G\times\text{diag}(kP)\times GT)\circ Vd$**Pin**=(**G**×diag(**kP**)×**G**T)$\circ$**Vd**
$Pin=(G\circ Vd)\times\text{diag}(kP)\times(G\circ Vd)T$**Pin**=(**G**$\circ$**Vd**)×diag(**kP**)×(**G**$\circ$**Vd**)T
$Pin=J\times Vd$**Pin**=**J**×**Vd**
where I**I** refers to the identity matrix and the matrix J**J**, termed here as the steady-state sensitivity matrix, is a dimensionless quantity. Matrix J**J** describes the quantitative relation between DC voltage variations and corresponding power flow variations.
Hence, in the ideal lossless model, increasing/decreasing the size of the DC droop constant in all HVDC terminals by a scalar constant will not have any impact on the steady-state power flow of the HVDC grid.
By following a similar procedure for the matrix $J-1$**J**-1, we get the relationships given by:
$\Delta Vd=J-1\times\Delta Pin\Delta$**Vd**=**J**$-$**1**×$\Delta$**Pin**
This indicates that, with increasing values of the scalar multiplier $\alpha\alpha$, the power flow pattern is affected more strongly by the DC grid line resistances (and hence by its topology). As a result, with larger values of $\alpha\alpha$, the balancing power distribution shows a larger deviation from the one predicted by the lossless analytical model. Since $\alpha\alpha$ and $kdkd$ are inversely proportional, larger values of $\alpha\alpha$ correspond to smaller values of $kdkd$ and vice versa.
Hence, we can conclude that, for smaller DC droop constants $kdkd$ applied to the HVDC terminals, the DC line voltage drops cause larger deviations of DC grid balancing power distribution from the estimation approach which ignores DC line resistance effects.

VI. Simulation Studies
A five-terminal VSC-HVDC network (shown in Fig. 3) was simulated using a PSCAD simulation software package. The simulation results are needed for checking the validity of the proposed analytical model, which estimates distribution of balancing power among different terminals, and for demonstrating the impact of DC line voltage drops in comparison to the ideal lossless analytical model.
Since much of the focus in this paper is on the MTDC aspect, the AC grids are represented only by aggregated models. Symbols used in Fig. 3 are listed here.
| Parameters of HVDC Terminals Used in the Simulation |

Symbol	Description
$VratedVrated$	Rated pole-to-pole DC grid voltage (in kV).
$kdkd$	DC voltage droop constant of the $ithith$ DC terminal (in per-unit).
$PmaxPmax$	Maximum (rated) power capacity of $ithith$ DC terminal (in MW).
$LijLij$	DC transmission distance between terminals ii and jj.

The parameters of the converter terminals used in the simulation are shown in Table II.
The set of values given in Table III was chosen arbitrarily to represent an initial steady-state condition for the MTDC system. In practice, this data should come from the power dispatcher (scheduler).
In order to get the desired power flow pattern, the unknown power at terminal 2 should be computed and used as the power reference for terminal 2.
Similarly, unknown DC bus voltages at terminals 1, 4, and 5 should be found and used as DC voltage references in the DC droop controllers of these terminals.
Terminal 3 is a constant power terminal of known reference value and hence does not need any more data. A short MATLAB code was written for solving the given DC load flow problem. DC load flow analysis of the given DC grid (i.e., Fig. 3) together with the desired power flow pattern (i.e., Table III) gives the set of numerical solution shown in Table IV.
The values in Table IV were used as power and DC voltage references in the respective DC terminals. Steady-state powers and DC bus voltages observed from the PSCAD simulation are shown in Table V.

Now, the power reference of terminal 3 is changed from 750 to 800 MW. This corresponds to a change of 50 MW.

TABLE V: PSCAD SIMULATION RESULTS WITH DC VOLTAGE AND DC POWER REFERENCES COMING FROM TABLE IV |

Terminal	DC Voltage (kV)	Power (MW)
1	500	750
2	510	750
3	520	800
4	530	750
5	540	750

The resulting steady-state power flow pattern after applying a change of 50 MW is shown in Table VI.

A. Comparison of Simulation Results With Estimation by Ideal Lossless Model

The total DC voltage response of the HVDC grid is given by:

$Vtotal=\sum i=15kdiPi,maxVtotal=\sum i=15kdiPi,max$

Substituting relevant values of $kdkd$ from Table II and the value of $Pi,maxPi,max$ from (33) into the expression of $VtotalVtotal$ in (18), we get:

$Vtotal$=0.00015×2000+0.0002×2000+0.00025×2000+0.0003×2000+0.00035×2000=2.15 kV$Vtotal$ =0.00015×2000+0.0002×2000+0.00025×2000+0.0003×2000+0.00035×2000=2.15kV

Decreasing power reference of terminal 3 by 50 MW (i.e., 50 MW) corresponds to the vector ΔP=[0,0,−50,0,0]ΔP=[0,0,−50,0,0] MW. Substituting this value of $\Delta P\Delta P$ and the value of $VtotalVtotal$ from (34) into (18), we find the estimated changes in nodal power flow shown in Table VII. The changes in DC bus voltages are estimated by (15).

TABLE VII: COMPARISON OF ESTIMATED STEADY-STATE CHANGES (BY LOSSLESS MODEL) WITH PSCAD SIMULATION RESULTS |

Terminal	Estimated Change in Power (MW)	Estimated Change in DC Voltage (kV)	Simulation Results Change in Power (MW)	Simulation Results Change in DC Voltage (kV)
1	-1.5	-1.5	-1.5	-1.5
2	-2	-2	-2	-2
3	-2.5	-2.5	-2.5	-2.5
4	-3	-3	-3	-3
5	-3.5	-3.5	-3.5	-3.5

From Table VII, it is evident that the ideal lossless model results in large errors in estimating the changes in DC bus voltages and nodal powers. It is also noticeable that, for terminals with droop control (i.e., 1, 2, 4, and 5), the estimation errors for change in power are nearly equal to the corresponding estimation error for change in DC bus voltage, suggesting that the DC bus voltage variations should be accounted for in order to accurately estimate the distribution of DC grid balancing power after the occurrence of power flow change at one terminal.

B. Estimation of Power Sharing by Proposed Analytical Expression

Now we try to estimate the power flow after a change in power reference of terminal 3 by 50 MW, but this time using the proposed analytical method which considers DC line voltage drops. In order to do so, we first have to compute the matrix $\partial P\partial V\partial V\partial P$. For the initial steady state given by Table V, the resulting Jacobian matrix JJ is given by (35), shown at the bottom of the page. This is computed by deriving the power flow equation of each node with respect to the DC bus voltage vector.

By substituting for $kdkd$ (from Table II) and JJ from (35) into (32), the matrix $\partial P\partial V\partial V\partial P$ becomes:

$$\frac{\partial P}{\partial V} = \begin{bmatrix} 0.00015 & 0.0002 & 0.00025 & 0.0003 & 0.00035 \\ 0.00015 & 0.0002 & 0.00025 & 0.0003 & 0.00035 \\ 0.00015 & 0.0002 & 0.00025 & 0.0003 & 0.00035 \\ 0.00015 & 0.0002 & 0.00025 & 0.0003 & 0.00035 \\ 0.00015 & 0.0002 & 0.00025 & 0.0003 & 0.00035 \end{bmatrix}$$

Multiplying $\partial P \partial V \partial V \partial P$ by ΔV=2.15ΔV=2.15 kV, we can find the resulting power distribution $\Delta P \Delta P$. The DC bus voltage vector $\Delta V \Delta V$ could be computed by (28). The estimated steady-state changes in DC bus voltages and powers from the analytical expressions are shown in Table VIII. The corresponding changes from the PSCAD simulation of the system are also included for comparison.

It is interesting to check the possibility that errors do not arise from the droop controllers not working properly. From Table VIII, it could be shown for all terminals that $\Delta P = \partial P \partial V \Delta V \Delta P = \partial V \partial P \Delta V$, both in the analytical and simulation results.

TABLE VIII: COMPARISON OF ESTIMATED STEADY-STATE CHANGES (BY PROPOSED MODEL) WITH PSCAD SIMULATION RESULTS, 50 MW

Terminal	Estimated Change in Power (MW)	Estimated Change in DC Voltage (kV)	Simulation Results Change in Power (MW)	Simulation Results Change in DC Voltage (kV)
1	-1.5	-1.5	-1.5	-1.5
2	-2	-2	-2	-2
3	-2.5	-2.5	-2.5	-2.5
4	-3	-3	-3	-3
5	-3.5	-3.5	-3.5	-3.5

The small estimation errors in Table VIII show that the derived analytical expression can indeed accurately estimate the steady-state changes of terminal powers and terminal voltages.

C. Impact of Size of DC Voltage Droop Constant

To observe the impact of the size of the DC voltage droop constant on load sharing, three droop constants (for terminals 1, 2, 4, and 5) were tested for the same step change in power of terminal 3 (i.e., from 0 to 250 MW). Simulation results are shown in Table IX. The sizes of the converters were kept the same as in Fig. 3.

It is shown in Table IX that, as the droop constant decreases, the balancing power distribution deviates more and more from the one predicted by the ideal lossless model.

D. Impact of DC Transmission-Line Distance

Due to the DC line resistance, terminals which are located further from the point where a change in power injection occurs (i.e., terminal 3 in the test case) observe smaller voltage drop at their DC bus. This describes why the changes in DC bus voltage at terminal 5 have been lowest in all previous cases. To further elaborate on this phenomenon, a similar change of reference (i.e., 250 MW) was tested for various lengths of the DC transmission line between terminals 4 and 5. The droop constant of terminals 1, 2, 4, and 5 was kept as *kdkd*. The results from the simulations are shown in Table X.

From Table X, it could be observed that the contribution of terminal 5 to DC grid power balancing decreases while the DC transmission distance between terminals 4 and 5 increases (compare the numbers in boldface letters). From this, it could be observed that HVDC terminals respond more strongly to power balancing demands occurring at closer distances than at further locations.

VII. CONCLUSION

In this paper, the impact of DC line voltage drops on the distribution of balancing power is thoroughly investigated. It has been demonstrated that the response of each DC terminal to the instantaneous balancing power demand is influenced by several key factors:

1. **DC Grid Topology and Line Resistances:** The layout and resistances of the DC grid lines play a crucial role in determining how power flows through the system.
2. **Location of Power Deficit/Surplus:** The location within the DC grid where a power deficit or surplus occurs significantly affects how the system responds and redistributes power.
3. **Value of the DC Voltage Droop Constant:** The setting of the DC voltage droop constant applied in the DC grid influences the terminal responses and the overall power flow pattern.

Due to these factors, the power flow pattern following a change in injected power at a DC terminal exhibits significant deviations from what is predicted by a simplistic lossless DC grid model.

An analytical expression for accurately estimating terminal power has been proposed in this paper. The validity of this analytical expression has been demonstrated through close agreement between the results obtained using the proposed method and those obtained from dynamic simulations applied to a five-terminal MTDC test model.

By taking into account the complexities introduced by DC line voltage drops, this study provides valuable insights into the behavior of MTDC systems and offers a more accurate tool for analyzing and predicting their performance in practical applications.

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